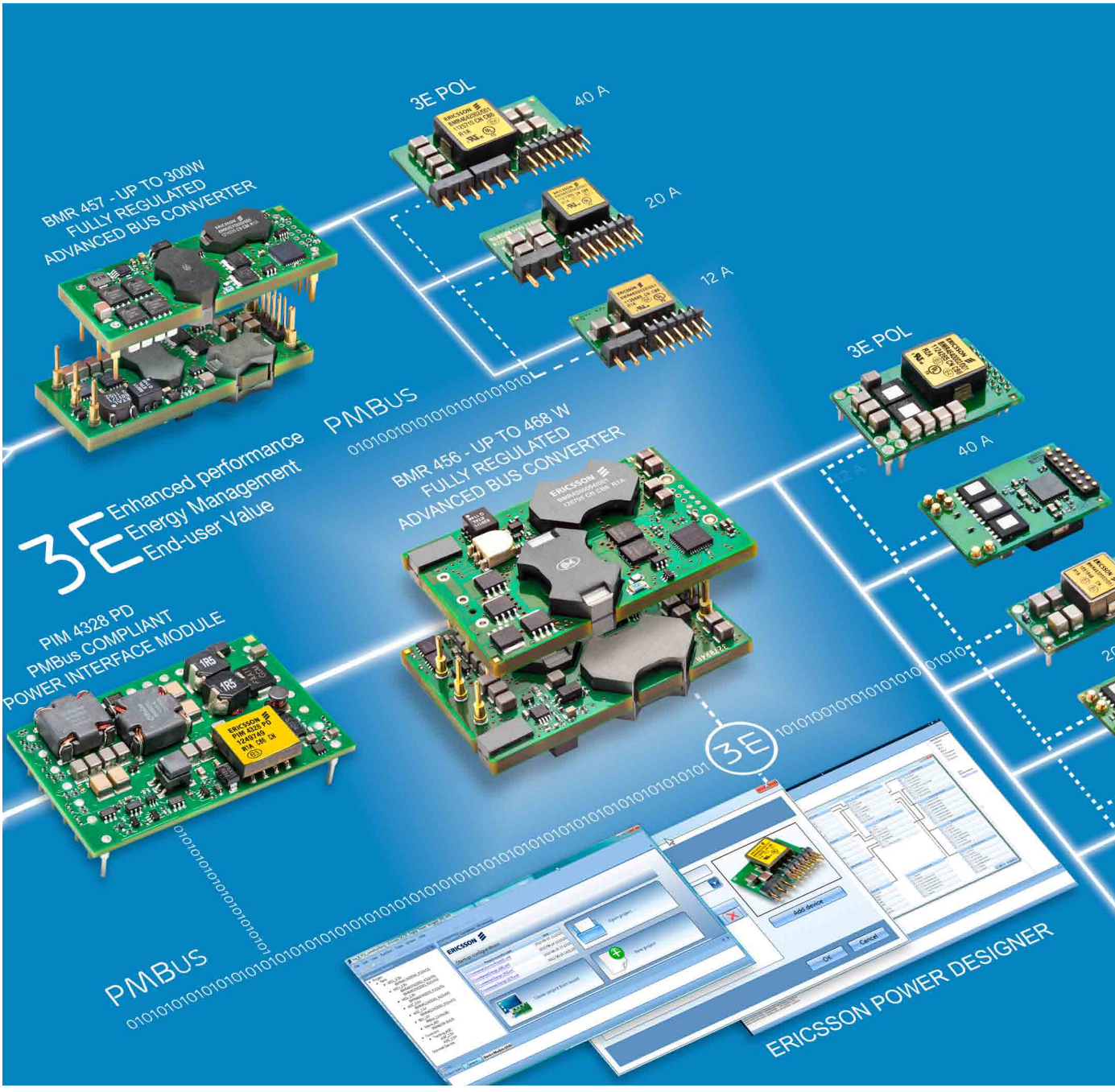
June 2013

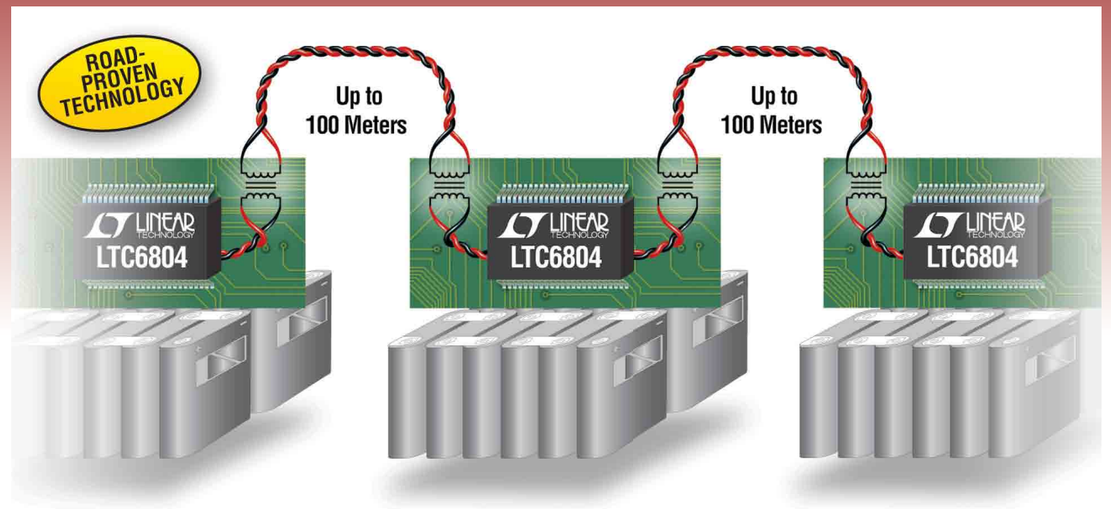
PSD EUROPE

Power Systems Design: Empowering Global Innovation



Special Report: Powering Consumer Electronics (pg 31)

1.2mV Accurate, Noise Immune Battery Stack Monitor



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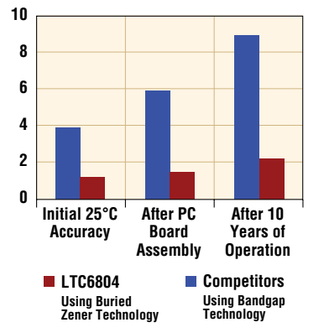
Measurement Error (mV) when Measuring a 3.3V Cell



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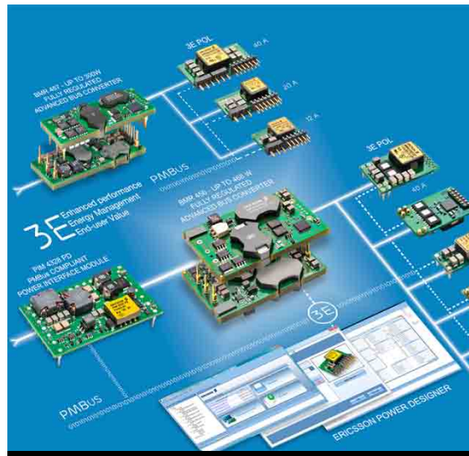
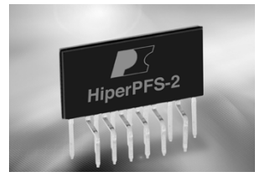


COVER STORY

Digital Power makes complexity simple (pg 14)



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Volume 10, Issue 5

Power's expanding intelligence

Each turn of the technology wheel brings with it new disruptions and new opportunities. In the area of power, the recent explosion of advanced microcontrollers has enabled designers and product manufacturers to put intelligent powered subsystems into applications where no controlled solution previously existed. This explosion of intelligently-powered subsystems brings with it design challenges on power management and system oversight only just now being addressed by the industry.

The Internet of Things
The Internet of Things (IoT) has shadings of meaning, depending on the person you are talking to and what market and application segment they are involved in. At this point IoT means more as a promise than as a reality, while companies incorporate cloud-based infrastructures into their existing processes and products. Once those systems start communicating more with one another, and the return on investment (ROI) becomes more apparent to the market leaders, those micro-nets of things joined by common application languages or service providers will eventually become a relatively seamless network of systems.

The challenge to the industry is to ensure that the systems, processes, and devices manufacturers develop have the scale- and flexibility to migrate towards a more cooperative communications, management, and data-sharing environment. Power efficiency in any IoT would be a paramount issue, as housekeeping activity cannot be allowed to impact device battery operating time to any significant extent, or take too much from the power budget in cable-tethered systems.

The Smart Grid
Means to interrogate and control a product's power usage will have significant impact on quality-of-life, especially in areas where large-scale waste of power by improperly operated and unnecessary loads is a problem. The ability for a power supply like a wall-wart to potentially interrogate its load via its USB connector, and communicate that information to the house's smart meter and thereby to the grid, will change the game in municipal energy efficiency from one of reaction to events to one of controlling events.

The rising number of continuously (or near-continuous) motor-driven applications in a home (and business) has increased significantly in the last couple of decades, and it isn't going to go down from here. Intelligent powered subsystems can enable more accurate power management from inside the product all the way up the grid.

Military
Military systems have a lot to gain from intelligent powered subsystems. From better team-served weaponry to individual soldier's gear, the systems both currently being fielded and those on the horizon are powerful force multipliers. The benefits of a battlefield of smart things may be restricted to whatever mobile ad-hoc network the systems are reporting to, but the commander of that battlefield would have a much greater level of intelligence and oversight from system telemetry of all major systems on a field.

Best Regards,

Alix Paultre

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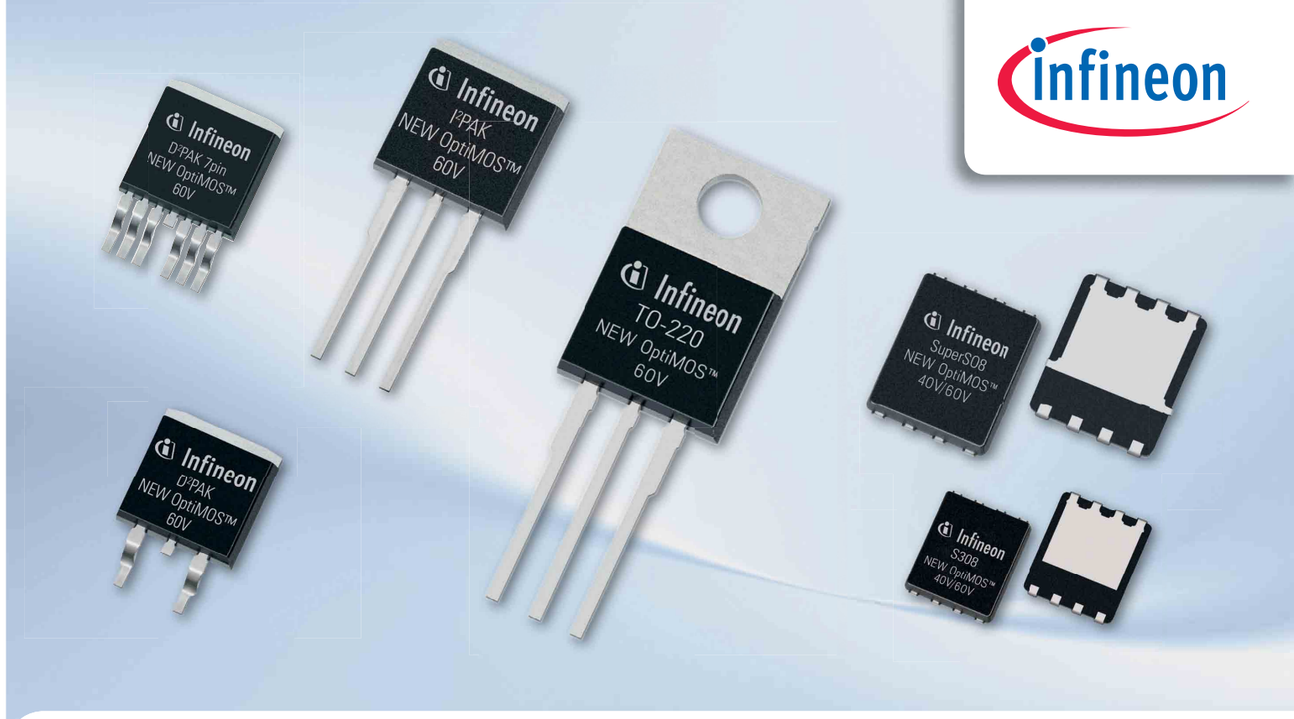

New OptiMOS™ 40V and 60V

Enables 96% Efficiency Level in Server Power Supply

Infineon's new OptiMOS™ 40V and 60V family is optimized for synchronous rectification in Switched Mode Power Supplies (SMPS) such as in servers and desktop PCs. These devices set the highest standards in power density and efficiency and at the same time reduce system costs.

The new OptiMOS™ 40V/60V families are also a perfect choice for a broad range of industrial applications like motor control, solar micro inverter and DC/DC converter like in telecom.

Key features and benefits of new OptiMOS™ 40V/60V

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- Highest system efficiency and power density
- Monolithically integrated Schottky like diode for highest efficiency

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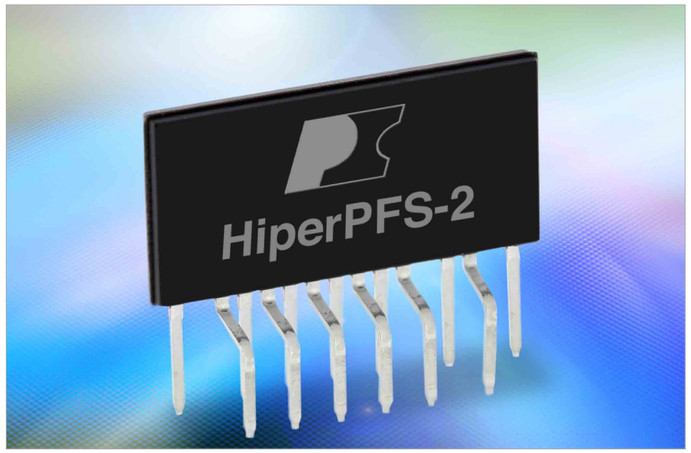
www.infineon.com/newoptimos

Highly integrated PFC IC addresses compact consumer products and computing apps

Targeting consumer devices and other mainstream product applications, the HiperPFS-2 family of high-efficiency, active-PFC ICs from Power Integrations serves offline applications from 100 W to 380 W. The devices combine a boost PFC controller, driver, PFC MOSFET, PFC diode and protection circuitry in a single package, enabling exceptionally compact designs and applications such as small-form-factor power supplies used in mini-tower PCs, all-in-one PCs, game console adapters and TVs.



The HiperPFS-2 controller uses a variable-frequency CCM algorithm, providing up to 97% efficiency across the load spectrum from 20% to 100% and power factor greater than 0.9 at 20% load with 265 VAC input for designs over 200 W. Including line-connected sense elements, the device contributes just 60 mW to a typical high-power adapter's 300 mW no-load budget. Conducted and radiated EMI are minimized due to the integrated a soft-recovery diode and a short parasitic inductance loop which results from the highly integrated, compact design.

According to Edward Ong, a product-marketing manager for Power Integrations, "we believe the HiperPFS-2 device is the most highly-integrated PFC solution currently available. This device enables designers to do things such as cost-effectively meet the 80 PLUS® Gold and Platinum efficiency standards in space-constrained PCs, for example. The device's excellent no-load performance simplifies design and reduces cost in high-power adapter applications targeting aggressive standby or no-load specifications."

Key applications for HiperPFS-2 ICs include TVs, PCs, game console adapters, telecoms and industrial products such as blowers, motor drives and chargers. A new reference design based on the HiperPFS-2 IC, RDR-294, describes a 350 W output power boost CCM PFC board with wide range AC input. RDR-294 is able to attain > 97% efficiency for 230 VAC across a wide load range and > 0.9 PF at 20% load.

HiperPFS-2 devices are sampling now in Power Integrations' innovative eSIP-16 package, which features an isolated metal heatsink pad for simple and easy clip mounting. HiperPFS-2 family devices are priced from $0.959 each in 10K quantities.

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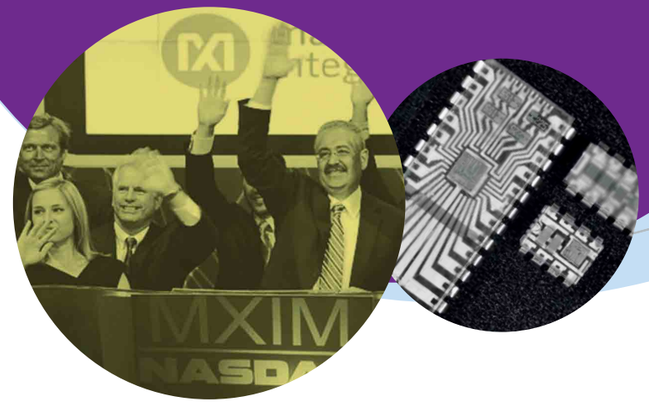
30 AMAZING YEARS



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Freescale Foundation to focus on STEM education

By: Andy North, Freescale Foundation

As the pace of technology continues to make steep academic demands on students and teachers across the globe, experts agree that the future workforce will need a standard literacy in technology in order to achieve success in engineering, science or math careers and to help develop the next generation of innovators. In response to these educational challenges and opportunities, Freescale Semiconductor announced the creation of the Freescale Foundation, a non-profit, 501(c)(3) organization focused on science, technology, engineering and math (STEM) education. Freescale will make an initial contribution of $5 million to the Freescale Foundation with plans for on going contributions.

"Our Freescale team is passionate about engineering and we want to bring that passion to our local communities with a desire to encourage the next generation of talent," said Gregg Lowe, president and CEO, Freescale. "Science, technology, engineering and math degrees lead to rewarding careers and to have the opportunity to inspire students is an amazing opportunity and one we take very seriously. The Freescale Foundation will help make it all possible."

The goals of the Freescale Foundation are to:

- Promote STEM learning at all levels of the education continuum
- Reduce the STEM education gap among women and under-represented populations
- Influence the development of the technical workforce of the future
- Strengthen Freescale's corporate citizenship and social responsibility.

"We are thrilled to put the power of Freescale's employees behind such a worthy effort," said Rick Morales, Freescale's director of Community Relations and Inclusion. "Though we know we can't do it alone, we think this is the right approach that will benefit our local and global communities. This is about doing our part to ensure that we can help develop the next wave of talented scientists, engineers and mathematicians."

Freescale has been working with educators around the world to bring the resources and solutions needed for advancing education, as well as provide sponsorships to deliver practical experience, for more than 30 years. The new Freescale Foundation will compliment the great work and success achieved over the last several years. The Foundation will continue to support our university programs as well as K-12 STEM education with resources, solutions, sponsorships, open source hardware, software and experience-based competitions, such as the Freescale Cup.

The Freescale Foundation will accept 2013 grant applications up until 30th August from qualified organizations that meet a certain criteria, including qualified organizations supported by Freescale's approximately 17,000 employees. The Foundation will focus on requests from eligible non-profit organizations in communities where Freescale employees live and work. Information on qualifications and open enrolment can be found at www.FreescaleFoundation.org and will be updated as more details become available.

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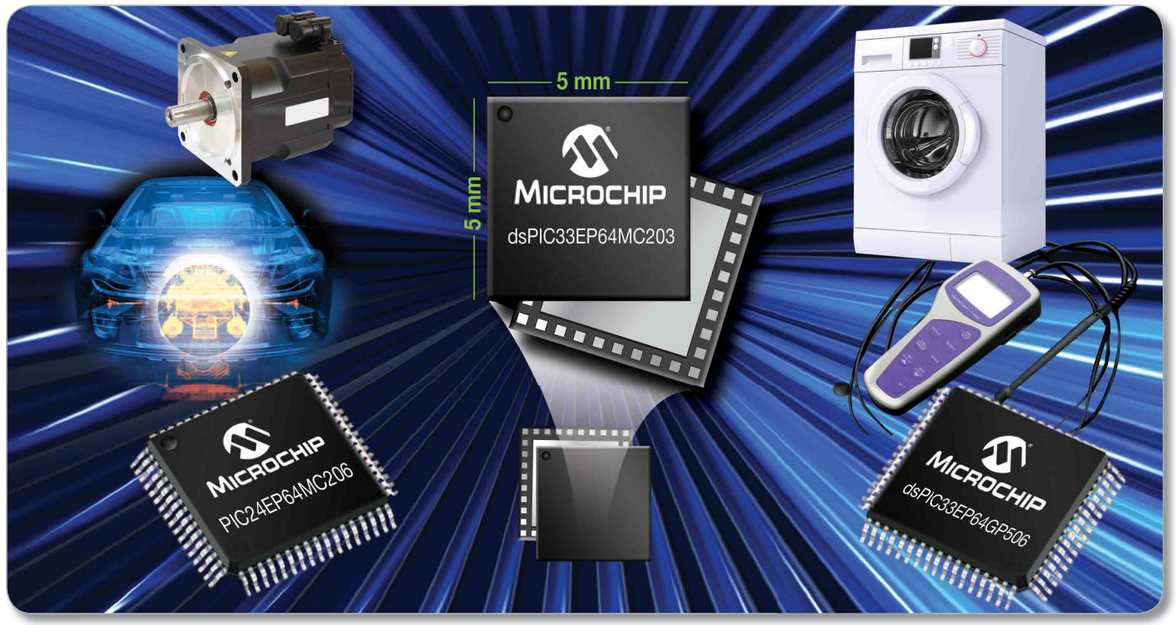
New 70 MIPS DSCs and MCUs offer more memory, plus temperature sensing and mTouch™ peripherals



With pin- and function-compatibility within the dsPIC33E DSC and PIC24E MCU families, Microchip is simplifying migration with Flash memory ranging from 32 to 256 KB and performance from 40 to 70 MIPS

Microchip's latest 70 MIPS dsPIC33E DSCs and PIC24E MCUs combine a wide range of Flash memory and performance options with specialised peripherals to cut the cost and size of your high-performance motor-control and sensing applications.

In addition to pin- and function-compatibility over 32 to 256 KB of Flash memory, they offer easy performance migration from 40 to 70 MIPS through code-compatibility with the dsPIC33F and PIC24F families. The new 'E' family of controllers also give you on-board op amps and a Charge Time Measurement Unit (CTMU) for on-board temperature sensing or mTouch™ capacitive touch sensing.

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Waste reduction in the portable charger market

By: Ryan Sanderson, HIS

Making portable electronic devices easier to use, but with greater functionality and a smaller footprint, are consumer-driven features which often lead to developments in the market. Those demands often result in challenges in electronics design. Increasing pressure for power hungry functions at a footprint, which allows for little increase in battery size, has resulted in the need for more frequent charging. This has led to concerns and demands regarding efficiency and waste.

The largest amount of waste is generated from the use of proprietary chargers for cell phones and other portable electronic devices. Usually when a device is replaced, the charger for the previous device becomes redundant. With close to 1.5 billion cell phones forecast to ship in 2013, the amount of waste generated is colossal. An initiative to solve this issue for cell phone chargers with a universal charging solution (UCS) is being driven by the GSM Association (GSMA) and a group of leading mobile operators. This wired charging solution uses a micro USB connector with the aim that the charger will be cross-compatible across different handset models, and eventually remove the need for a new charger to ship with each handset. By the end of 2012, a majority of handsets had adopted micro USB as a common connector, though no operators have yet removed the charger from new handset shipments. Despite this, IHS believes that the initiative will drive a decline in the percentage of new handsets shipped with a charger to just 40% in 2017, resulting in a decline in the cell phone charger market of $700 million compared with the market 2013.

At the end of October 2012 the International Telecommunications Union (ITU) also announced a new Universal Power Adapter (UPA) standard, aimed at home communications equipment such as modems, set-top boxes, home networking equipment and fixed telephones. The similar initiative also aims to cut down waste by reducing the number of redundant chargers.

With traditional markets projected to experience large declines, charger manufacturers are looking for new opportunities. For some the solution has been as simple (in concept) as removing the wires. Wireless charging, in particular inductive charging, is starting to become more popular. Samsung, Nokia and HTC have all released or announced handset models with wireless charging built in. Apple announced earlier this year that its iPad 5 will contain wireless charging capability via a protective cover and Toyota and Jeep have also announced that 2014 models will contain built-in wireless charging options. IHS projects that the number of wireless power transmitters (chargers) shipped will grow to more than 200 million in 2017, driving a market of $5 billion.

Ironically, wireless charging is actually less efficient than charging via a wire, though the solutions from wireless power and charging manufacturers are not only to provide a convenient method for consumers to charge portable electronics at regular intervals, but to also provide a universal solution that is compatible with many different devices own proprietary charger.

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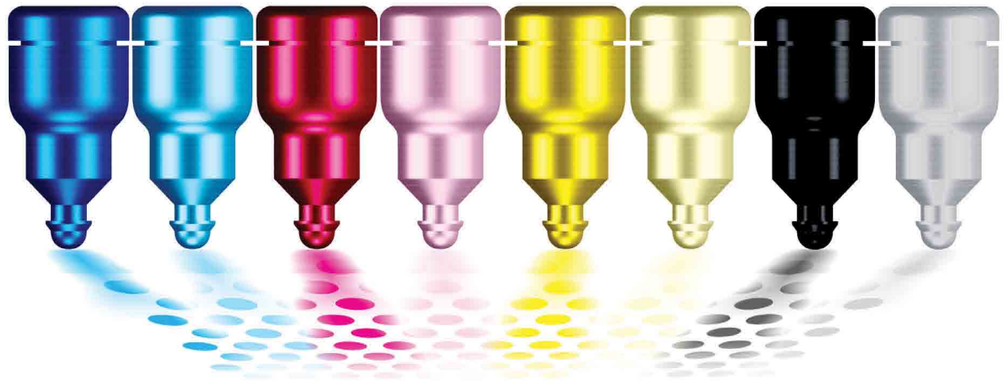

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MP103FC Power Amplifier: Dual-Channel Design Delivers Space Savings, Cost Savings

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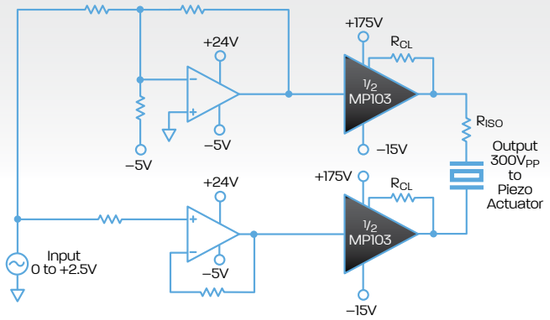
The MP103FC from Apex Microtechnology is a dual-channel power amplifier that is designed to drive multiple loads with a single device. With full power bandwidth rated for 230 kHz, the MP103FC is optimized for industrial applications requiring piezoelectric loads with more than one driver. This thermally enhanced module also features output current of up to 15 A PEAK per channel and a 30 V to 200 V power supply. A single MP103FC delivers high current, high voltage and high speed at a per unit cost savings that makes it the option of choice versus single amplifier solutions and discrete designs.

- Print head electronic drives for industrial ink jet printers



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Flyback power supply development: Part V

By: Dr. Ray Ridley, President, Ridley Engineering

This article is the fifth of a series in which Dr. Ridley shows the steps involved in designing and building an offline flyback converter. With full input voltage and full load applied, the control-to-output transfer function and loop gain is measured and compared to predictions.

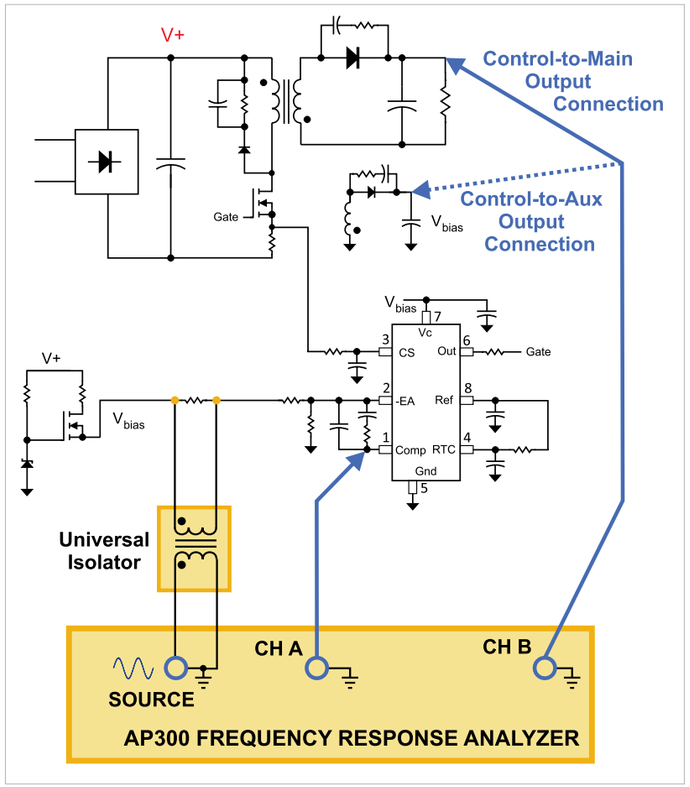

Figure 1: Schematic of the flyback converter with AP300 connections for measuring the control-to-output transfer functions.

Theory and Practice

The late and great analog guru Bob Pease had a quote, which is always good to remember when designing power supplies:

"In theory, theory and practice are the same. In practice, they are different!"

I have been designing and measuring power supplies for over 30 years now. I don't recall ever meeting one power supply that didn't surprise me when testing it and making measurements. In this article, we will see how the measurement of a multi-output power supply does not conform to the predicted results, proving Bob's theory above.

Flyback Converter Control Measurements

Figure 1 shows the schematic of the flyback converter ready for small-signal measurements. The AP300 frequency response analyzer was used to inject a signal into the circuit across the 20 ohm resistor. The output signal from the AP300 was isolated with the Universal Injector, a wide-band transformer capable of injecting into control circuits from 0.1 Hz to 30 MHz [1].

When making control measurements of power supplies, it is commonplace to start the sweep frequency at 10 Hz, and stop at twice the switching frequency. Control information above half the switching frequency is of limited use, but it is helpful to be able to sweep past the switching frequency with an analyzer in order to verify its operating point. The lower frequency of 10 Hz is chosen since it is very important to verify that a converter has the proper gain at line frequencies and their harmonics. With a current-mode converter, the gain in this region can be very high, and the AP300 excels at measuring in this region of operation.

Channel A of the analyzer is connected to the output of the error amplifier of the control chip (Comp Pin 1), and Channel B is connected to either one of the two outputs of the power supply. In theory, these two points will track each other quite closely, but as we will see, this does not always happen in practice.

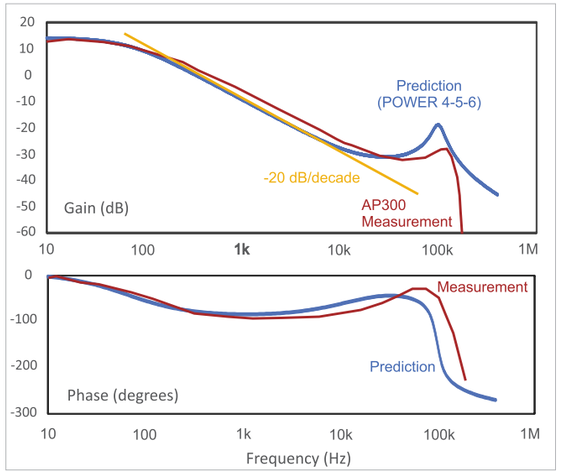

Figure 2: Prediction and measurement of the control-to-Main-output transfer function.

Figure 2 shows the theory and prediction of the control-to-output transfer function for the flyback converter. In this measurement, Channel B of the AP300 was connected to the main output of the power supply. The auxiliary output was loaded with 30 mA as described in Part IV of this series of articles.

The blue curve of **Figure 2** shows the control-to-output transfer function predicted by POWER 4-5-6 [3]. The red curve shows the actual measurements. As you can see from these two curves, there are significant discrepancies in the gain after 100 Hz or so, and again at half the switching frequency. This is quite normal for the first attempts at measuring and reconciling with models.

The modeling can be refined by incorporating the actual value of power supply output capacitor from measurements, and changing the predicted frequency to match the measured frequency. However it should be noted that in real-world power supplies, it is common that the measurements and predictions have deviations, and those shown in **Figure 2** are actually in quite good agreement compared to what you may see on your particular power supply. It is one of the reasons that empirical measurements should always be done on a power supply. Models are often of limited accuracy in such a high-noise environment

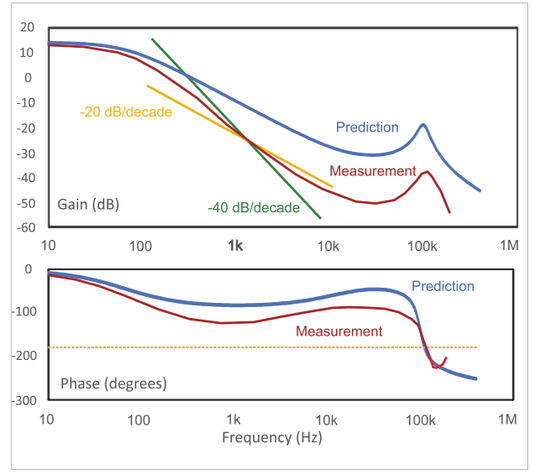

Figure 3: Prediction and measurement of the control-to-Auxiliary-output transfer function. There are substantial unexplained discrepancies.

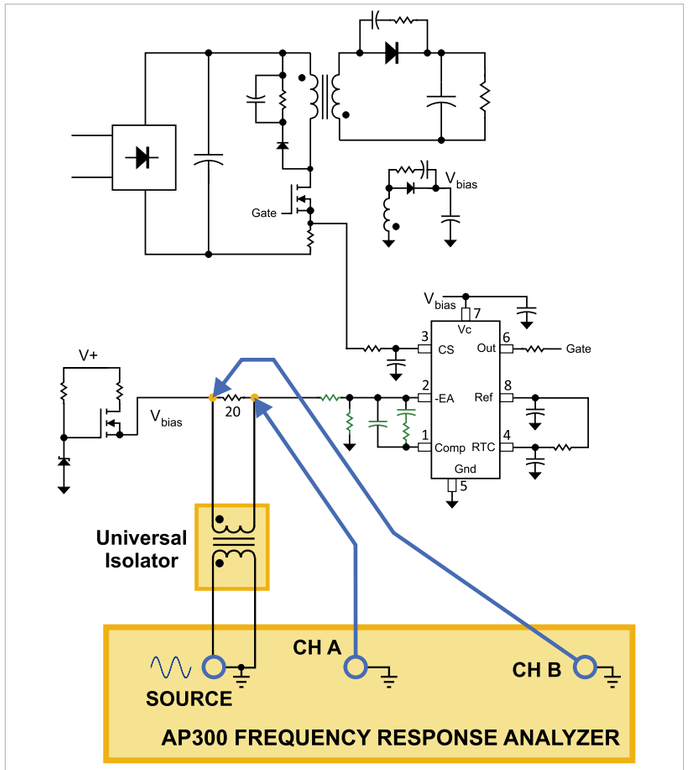

Figure 4: Loop gain measurement setup using the AP300 analyzer.

with nonlinear switching power supplies.

The gold curve of **Figure 2** shows a -20 dB/decade slope asymptote. This illustrates that both the measured and predicted transfer functions roll off with this same slope, as would be expected for a current-mode system.

Control-to-Auxiliary-Output Measurement

The desired feedback point of the converter is not the main output, but the auxiliary output. If feedback can be taken from this output, the converter can be regulated without the use of an extra feedback amplifier (such as a TL431) and optocoupler. For low-cost bias supplies, and for high-reliability supplies, elimination of these parts is important.

In **Figure 1**, Channel B of the AP300 analyzer connected to the auxiliary output feeding the bias of the control chip and the feedback compensation network. **Figure 3** shows the result of the auxiliary output measurement. There is now a very substantial difference between the measured and predicted transfer functions. At dc, the predicted blue curve and the measured red curve are in close agreement. However, once the first pole is reached the curves separate quite drastically, and at 10 kHz there is over 20 dB of difference between the two curves!

Two asymptotes are shown on the gain curve of **Figure 3**. It can be seen that the measured gain does not correspond to either a -20 or -40 dB/decade slope, which is quite an unusual result.

There are no models to explain this kind of deviation. It is not particular to this specific flyback converter, but this kind of event occurs with every converter with multiple outputs. It was observed in the coupled-inductor forward converter in reference [6].

Loop Gain Measurement

The deviations from predicted results also show up in the loop gain measurement of the flyback power supply. **Figure 4** shows the test setup for measurement of loop gain with the AP300. The injection technique is exactly the same as in **Figure 1**, but the test points are changed.

With this setup, the loop closed around the auxiliary output was measured, and the results are shown in **Figure 5**. As with the control-to-output measurement, there are very substantial differences between the prediction and the measurements.

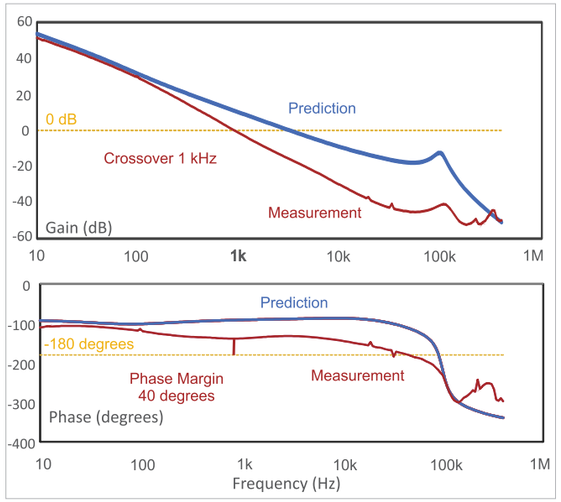

Figure 5: Loop gain measurements versus predictions. The discrepancies in the control-to-output measurement also affect the loop gain result.

There are a several design choices you have when running into this kind of situation. You can abandon the proposed control scheme of running off the auxiliary output, and go with something that adheres closer to predictions. Or, you can ignore the predictions, and just design the converter based upon the actual measurements. This is the most usual approach taken in industry since saving parts cost is usually more important than getting good agreement between measurement and theory.

If you are doing high reliability work where intense worst-case analysis is required, the multiple-output converters obviously present problems with predictability. Running a series of measurements is not a guarantee of ruggedness if there is no explanation of the parameters of the power supply causing the discrepancies.

Summary

The fifth part of this series on flyback circuit design highlights the issue of discrepancies between predicted and measured control characteristics for multiple output converters. This is a very important issue that has not been thoroughly addressed by researchers.

However, it is just one of the issues of converter design that make it such a challenging field. There are so many nonlinearities and parasitics involved in the control characteristics of power supplies, it is quite common for behavior to be unpredictable. In this case, it is essential that comprehensive measurements are made on multiple converter prototypes before a design is put into production.

While the flyback circuit is a simple example of this kind of event, it can also be observed with much more complex power circuits, such as the LLC converter. Measurements are crucial as the complexity goes up since the circuit models are so often lacking in accuracy.

www.ridleyengineering.com

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Digital Power makes complexity simple

On-demand content services are among the factors driving mobile data

By: Patrick Le Fèvre, Ericsson Power Modules

The number of mobile broadband subscriptions has grown by around 45% year-on-year reaching 1.7 billion in 2012, according to data released in the latest Ericsson Mobility Report . In addition to this growth, there also is steady progress in the amount of data usage per subscription. The changing habits of people and the way in which they use networks, increasingly using on-demand content services for example, is driving this increase in mobile data. This combined with the growing deployment of the high-speed internet infrastructure via fiber-to-home means that manufacturers in ICT (Information and Communications Technology) applications are being required to develop ever higher performing and higher capacity equipment in a shorter time-to-market, while also implementing the latest hardware and software technologies to ensure low energy consumption.

While this is an extremely challenging situation, it also generates many opportunities to develop new ways of managing board power. For example, moving from passive 'Board Mounted Power Sources' (BMPS) that only supply power to loads, to very advanced combinations of hardware and software that make a contribution towards the full integration of board power within the digital chain.

Figure 1: Ericsson's high-end subscriber management and routing board

Pushing the limits

The challenge for the board power system designer is to predict what will be required in terms of increasing power, decreasing board-space, higher flexibility and lower power consumption by the final end-application network data processor. Leading-edge equipment designed to handle high levels of data traffic is often based on multiple cores or processors that are not always fully available at the time of system development. And this equipment requires highly sophisticated power management with power sequencing, monitoring and the capability to dynamically modify an element of the power scheme to adjust to traffic conditions and thereby enable a reduction in energy consumption. An example of this type of complex equipment – an Ericsson high-end subscriber management and routing board – is shown in **Figure 1**.

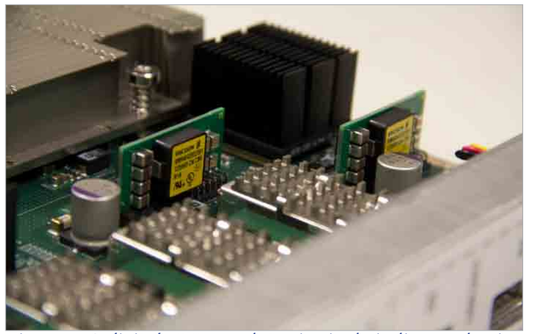

Figure 2: A digital POL regulator in single in-line packaging saving board space and improving cooling

These types of demands are not entirely new and the BMPS industry is actually quite used to this type of situation. It often faces a wide divergence between the preliminary specifications issued by systems designers and the final end application. And in high-end data processing world, this divergence in terms of power demand and flexibility is reaching an unprecedented level. The time-to-market to support network expansion is becoming ever shorter, while the increase of computing power per network controller is running at a similar rate. Board system architects therefore often find 'moving goalposts' when estimating power demand via simulation to match the power required by the actual end application when the system processors reach production maturity.

Complex sequencing is fun

Because network-processors are very complex – and each new evolution integrates more functionality – the current required by the processor could increase by up to 60% from the preliminary specification of the processor to the mature version. Clearly, an evolving processor makes it difficult for board power designers to define the most efficient power architecture for the application.

In addition to the increase of power required by the processor, revision after revision, the voltage sequencing is crucial and also has to evolve in step with the development of the processor. This means that designers will have to reset the voltage-sequencing scheme with each new revision.

Furthermore, as well as the power and sequencing plan, when the board is finally released, during the lifetime of the equipment, network processors will be subject to firmware upgrades that may require different sequencing values to optimize operation and reduce energy consumption. In this type of application it is problematic in the extreme to use conventional power architectures, such as implementing analog point-of-load (POL) regulators with a sequencing setup via physical resistors, which will require

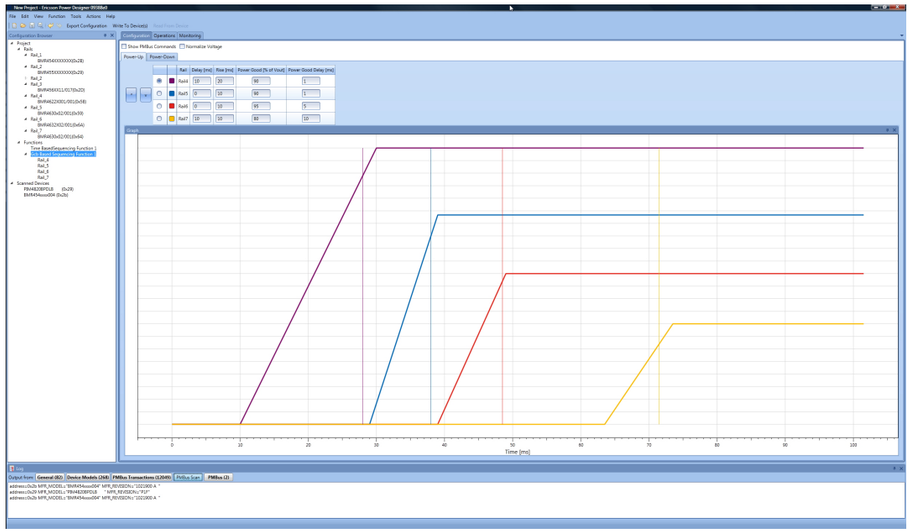

Figure 3: Ericsson Power Designer sequencing

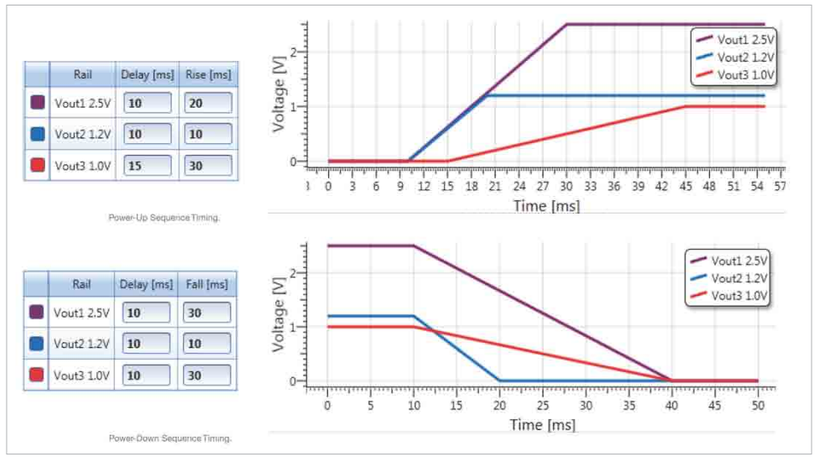

Figure 4: Time-based sequencing – Rise-time and fall-time

hardware modifications and make lifetime upgrades almost impossible.

To solve the complex equation of setting the power architecture in parallel with the application development, and to guarantee full lifetime optimization, board power designers are increasingly implementing digitally controlled power architectures that combine digital POL regulators. These can be paralleled to achieve the level of power required by the processor (**see figure 2**), in conjunction with the flexibility offered by programming the setup sequencing using software such as Ericsson Power Designer (**see figure 3**), which makes it possible to create specific configurations for power rails and to modify configuration at any time without requiring hardware changes.

Because varying type of processors and other strategic components such as memories require different types of sequencing on the same board, power architects have often to set up different sequencing schemes, such as Time Based, Event Based, Group Communication Bus Based and Voltage Tracking. As shown in figure 3, setting parameters for any type of sequencing is very simple and can be achieved via software. The example presented in **figure 4** shows time-based sequencing in which delays, rise-time and fall-time are based on processor specifications.

In this configuration, the 1.0V core voltage must ramp slowly over 30 milliseconds, while the auxiliary voltages ramp up earlier – within 10 milliseconds – to power supervisory functions, ensuring they are operating before the core turns on. During the shutdown, all voltages are switched off at the same time, within 10 milliseconds; however, the fall-time is adjusted to guarantee smooth transition until all functions are switched off.

As mentioned previously, during the design of the equipment, parameters are evolving and, in case of any different required sequencing, power architects can simply modify the value and send a set of commands to load into the POL or a new configuration file into the Board Power Manager in only a few minutes. The same is possible when the system is in operation and a firmware update that requires different voltage sequencing is recommended for performances optimization.

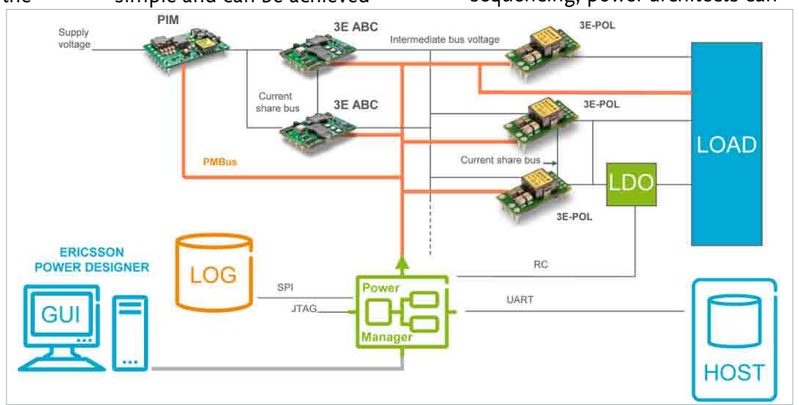

Figure 5: System overview

As shown in **figure 5**, systems using digital power architecture are extremely flexible and the site manager can access any part of the board, down to a single POL through the digital interface.

Powering the core while saving energy

Over many years the semiconductor industry has drastically optimized energy usage with built-in processor energy management that has significantly improved performance and reduced energy consumption. We all see the benefits of this in our smartphones, tablets and laptops. However, the high-end processors used in data networking have increased their computing power to reach more than 300-Mbps throughput and the number of cores per processor is increasing and beginning to push the limits of Moore's Law. An increasing number of cores and more power requires ever-shrinking process technologies, resulting in lower voltages and higher currents.

Core voltage is now in the range of 1V and below, with current up to 90A per processor operating at full capacity, but at 10A and below, when operating in a lower utilization mode. To power processors efficiently, power designers are exploiting another benefit offered by digital power, which is to connect a number of digital POLs in parallel. For example, implementing three 40A POLs to guarantee 100A across all conditions and using the benefits of phase spreading to decrease ripple and noise at full power and phase shading to reduce the number of POLs in operation when not required. Although usually complex to manage, the implementation of this type of functionality with digital POLs makes it very simple in practice.

Figure 6 shows how phases can be adjusted when using Ericsson Power Designer. As for the sequencing shown previously, phase spreading and phase shading can be simply

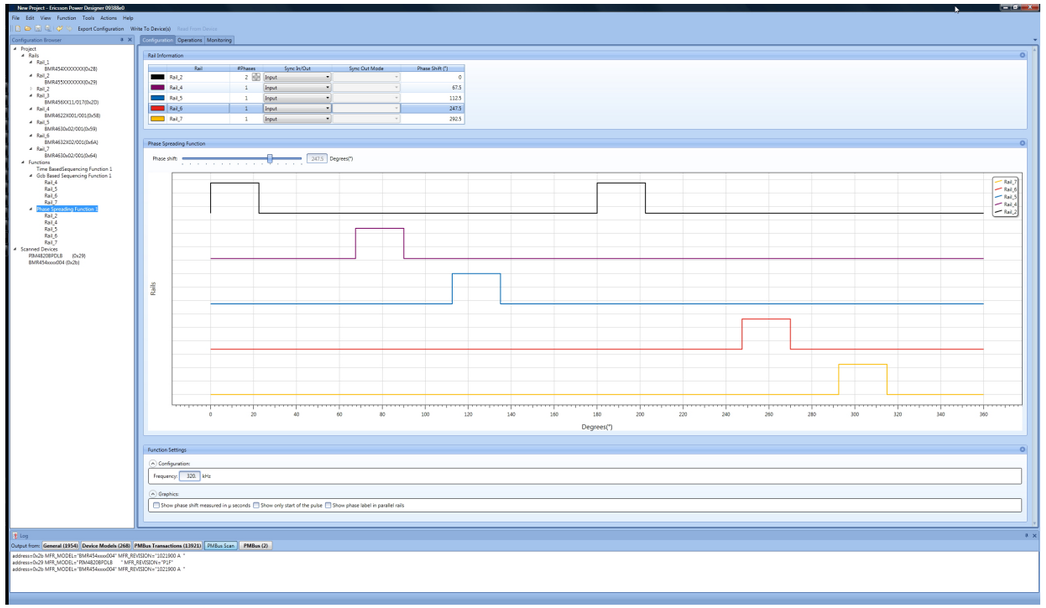

Figure 6: Phase spreading

programmed. In addition, systems architect can develop multiple configuration files to meet certain profiles that can be called up by the board power manager from local storage. In some applications, the processor directly communicates with the board power manager to set the number of phases required for optimized performances and how those phases should be shifted or synchronized. This simple example provides an idea of the huge potential offered by digital POLs directly communicating with the master processor.

Monitoring and energy reporting
Energy regulations and the growing importance for network operators to reduce energy consumption are adding to the demands upon board power designers to report the power consumption of each board, which requires additional current sensing and other circuitry. As described in the May issue of Power Systems Design, systems architects working on Advanced Telecom Computing Architecture (ATCA) applications are implementing Power Interface Modules (PIMs) with a built-in PMBus controller that is able to monitor current consumption at any time of operation and to report accurate power measurement. The implementation of PIM technology is now spreading to larger number of applications in addition to the ATCA segment.

Current monitoring via the PMBus is available via any digital power module, isolated or non-isolated, simplifying energy monitoring and offering the possibility to supervise the overall system. Digital power modules also include a large number of alarms that can be programmed to report deviation from any default, in addition to temperature monitoring. While it is a clear advantage to know the temperature of the Advanced Bus Converter or POL regulator, the real benefit is to help systems managers to diagnose any abnormal deviation before reaching alarm level. Abnormal deviation from calibrated configuration could easily be the sign of forthcoming failure, trigging a request for preventive maintenance and therefore avoiding traffic disruption and loss of revenues.

Board space saving and temperature mapping
In addition to reducing time-to-market and energy consumption, saving board space to accommodate additional data processing capability is another challenge faced by systems designers. This often comes with another challenge: that of limiting the airflow bottleneck and optimizing cooling to achieve the highest performance from the network processor without overheating.

Saving board space is often achieved by implementing vertically mounted single in-line POLs. In addition to highly efficient power conversion, additional monitoring features built into digital POLs, such as current, voltage, temperature, alarms, parameter settings and many others that are therefore no longer required as separate functions, represent a significant board saving, thereby freeing space for additional computing power.

Gathering temperature information from a large number of points within a board can also be used by systems managers to create a thermal picture of the complete board, which besides detecting early failure is also used to adjust cooling to what is required by the system. In previous generation of systems, thermal mapping relied upon a network of thermocouples requiring additional circuitry, calibration and complexity, which can highly be simplified when implementing digital POLs with this built-in functionality.

If we consider the high-end subscriber management and routing board shown on **figure 1**, we can see that the digital POLs (with the yellow stickers) are widely distributed around the board and, understanding that the airflow circulating between and across the heatsink and over the POLs, it is obvious that thermal data collected by each POL represents valuable information for systems architects looking to optimize overall board cooling.

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Crucial selection criteria for an AC/DC supply

There are many tradeoffs in selection which complicate the process

By: Don Knowles, N2Power

Naturally, when specifying an AC/DC supply for a new project, one needs to select a product with the right output voltage and current rating, as well as input voltage range. But it goes much deeper than this in reality. There are two major issues to be addressed: What is the power-distribution topology that will be used? And what are the thermal and supply placement/mounting options?

Without going deeply into the internal topologies of the AC/DC converters, there are some commonly used design approaches, but to the end user, the supply can be considered simply as a "black box" with input, output, and performance attributes.

If all that's needed is to supply a single DC rail to a single PC board from the AC supply, this is a relatively easy situation. For example, it may be required to deliver 12V DC at 20 A (nominal 240 W) to a mid-size board, with all further power needs handled locally on that board. Many applications, however, need that single voltage across two or more boards, or need different voltages (and currents). Right there, you have the choice of one larger supply, or multiple smaller ones, **Figure 1**.

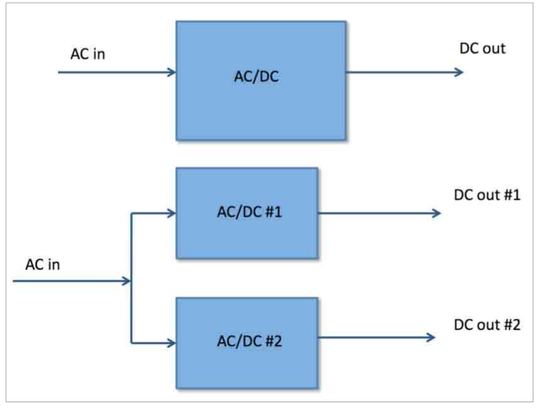

Figure 1: The AC line can feed a single larger AC/DC converter (top), or several smaller ones (bottom)—even with the same output voltage.

Many applications use multistage-power-distribution approach, where the AC/DC supply feeds one or more intermediate bus converters (IBCs), which in turn transform the DC voltage from the AC/DC supply into lower-voltage DC rails. For example, individual IBCs may take 48 VDC and provide 12 V DC, 5V DC, 3V DC, and other voltages needed by the circuitry, **Figure 2**.

If the system uses IBCs, the decision for which AC/DC converter would be needed is again simplified. In most designs, there is only a single intermediate voltage, such as 48V DC or 12V DC (some more complex systems use a variety of IBCs supply rails. Therefore, the focus should be on finding an AC/DC supply (or supplies) which provides the desired intermediate rail voltage(s), at sufficient current.

Efficiency
Efficiency and the thermal load dissipation have major effects on design and placement, as well as operating and life-cycle costs. Many regulatory standards now mandate minimum supply efficiencies, with the specific value depending on the nominal wattage rating of the supply. The good

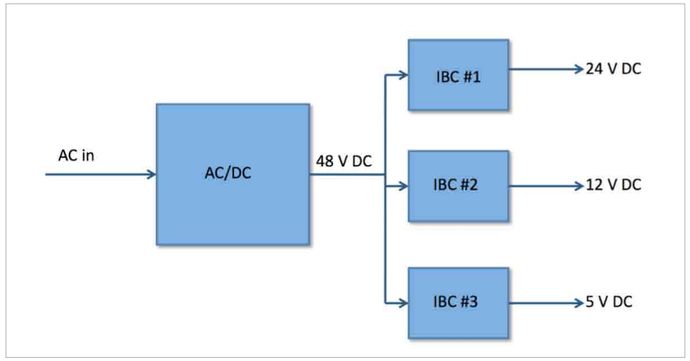

Figure 2: Many installations use a single AC/DC converter to supply a one DC voltage to an array of intermediate bus converters, which in turn provide the final DC rail voltages.

news is that almost any supply from a reputable vendor will meet these standards. But it is important to make sure that the supply is certified for the countries in which the product will be used, since these standards are not fully harmonized.

Given that almost all new AC/DC supplies have efficiency in the 85 to 95% range, why should we be concerned about exact figure? After all, today's switching supplies are a big improvement over the 50-60% efficiency of older, linear (non-switching) supplies.

Here's why: even a few percentage points can make a big difference, three ways. Using an example of a casino floor of several hundred gaming machines:

- First, we need to supply that extra power, which adds up and is an ongoing cost.
- Second, we need to get rid of the heat that the supplies generate; again, an ongoing cost.
- Finally, heat is the killer of electronics, and even a few more degrees can severely shorten the life of a supply—which means field replacement, labor costs, and a product not generating revenue for hours or longer.

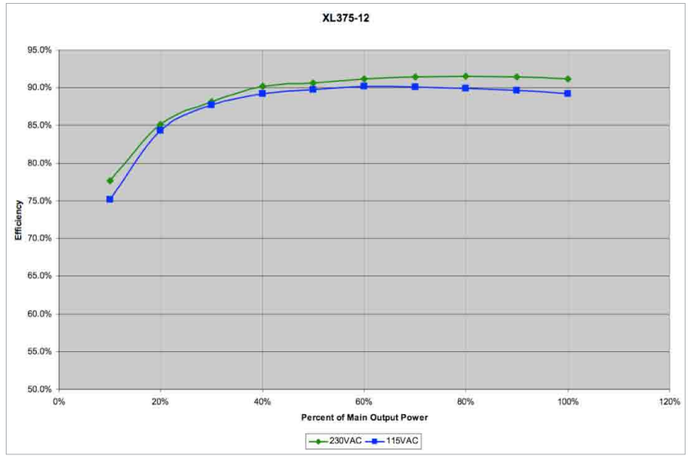

Figure 3: A supply's efficiency is not constant, and varies with load; each supply has an important region where its efficiency is at a maximum. [From Figure 3-1 "Typical XL375-12 (12V, worse-case) Efficiency Curves", shown in Product Specification XL375 Series 375-Watt AC to DC Power Supplies, available at http://www.n2power.com/704601.pdf]

It is important to note that a properly designed and built supply and operating within its rated specifications has a MTTF (mean time to failure) of several hundred thousand hours—but a 10°C increase can cut the MTBF in half.

So what is the solution? Choose the highest-efficiency supply you can afford in BOM cost, and also factor in the operating and lifecycle costs. But be careful with efficiency numbers, as they are not constant across the entire load range. Most vendors provide an efficiency vs. load graph, which shows the supply's performance from light load—say, 10%—to full load. Supplies usually have an efficiency "sweet spot" at around 85-95% of their full current rating, **Figure 3**.

Understand the position on the load curve, and the product's duty cycle, to decide how much efficiency is needed and the benefits of the cost of additional efficiency. A supply that is operating mostly at mid-range load (50%) and 85% efficiency, and only occasionally at near-maximum load (90%) but with much higher efficiency of 95%, would cost-out differently than one which is slightly less efficient (such as 93%) at 90% load, but operating at that point most of the time. The up-front cost for a few extra points of efficiency may not be worthwhile or even meaningful, depending on the product's operating modes.

Similarly, it is important not to over-specify the supply's size, with the intention of getting greater efficiency and longer life.

Figure 4: A supply such as the XL375 from N2Power offers various built-in protection modes that would be difficult to add externally.

For example, if we need a supply that can deliver 400W, we would look for a supply that is rated in the 500W range. It could also be possible to get a 1000W supply, which would certainly have more capacity than needed. However, it would be less efficient than a 500W supply, in paying more for the supply itself, and the operating costs will be higher.

Location

Where it's located, is a major factor in success. Some supplies are designed and specified for convection cooling alone, and no forced airflow; others assume active cooling via airflow (usually from a fan, but chillers are also used in some cases). Other passive cooling techniques include heat sinks, heat pipes, and cold plates, all of which add to cost and design complexity.

In general, having forced-air cooling allows a less-expensive supply design, but one must factor in the cost and reliability of the fan itself. The supply vendor will specify how many cubic feet per minute (CFM) of air, and at what temperature, is needed to push past the supply.

Whether using passive or active cooling, consideration of the location and orientation of the supply is important. Most supplies are rated at a defined orientation, and changing this means that heat-generating components will have inadequate airflow (and also heat adjacent components). If there are any questions regarding mounting and its impact on the supply's ratings, this will need to be taken up with the vendor for additional insight.

The reality is that supplies tend to be dropped in an available, crowded spot—often next to other sources of heat, such a PC boards with hot processors, or motors. The ambient temperature expected can be much higher than what the PSU actually encounters, so it is vial to clarify where the dissipation of the non-supply part of the system is going and how it gets there. This may have to take this into account as part of the cooling strategy or supply-rating assessment.

Electrical specifications

Now, we can focus on the electrical specifications. Start with the AC side of the AC/DC converter, of course, and a straightforward question about the AC line's nominal value and range.
Will the AC line be only 120 VAC only, 220 VAC only, or is it required to handle both nominal lines with a single supply? In general, supporting only one AC range results in a less costly supply, but the difference is fairly small with most supplies. Some vendors do not even offer units for a single line range, since it's a logistical headache to design, qualify, and ship two similar supplies.

The bigger question is the line tolerance needed. The wider the tolerance around the nominal value—5%, 10%, or more—the more difficult the supply challenges, especially when it is called to supply maximum output at minimum line; note that a full-range supply could be specified for 90 to 264 VAC. Also, on-going line voltage fluctuations make it more difficult for the supply to maintain its regulated output, even if the load is not changing.

As with most engineering designs, it's these cases of operation that require a careful study of the vendor's data sheets, and see if max/min specs are maintained under worst-case conditions, or only at nominal points.

Moving on to the DC side, look at required voltage(s) and associated current rating(s). Do check if the supply's output regulation meets design requirements—that's the ability to maintain the nominal output within tolerance, despite shifts in the current being drawn from the supply.
Most vendors offer screw terminals for the DC output, but connectors are also available as standard options. Screw terminals reduce costs of interconnection cables, but require more labor in final assembly of your product and are prone to wiring errors.

Other features need to be checked are on the regulatory compliance. The major ones cover efficiency; power factor correction (PFC) (how much the supply shifts the line current with respect to voltage); safety issues such as isolation and fault modes; RoHS (reduction of hazardous substances); and EMI (electromagnetic interference). Check that the vendor meets the applicable standards and certifications; as nearly all do.

If not, just go to another vendor because there's little one can or should do if the supply falls short in any of these areas. Even if you something could be done, there's no way to qualify the fix and get certification, so any engineering effort would be wasted.

Nearly all supplies, such as the XL375 series from N2Power (**see Figure 4**), incorporate standard protection features such as overvoltage protection (OVP), output current limiting and shutdown (crowbar), and thermal shutdown. This supply offers shut down on command, loss of input power, or whenever excessive loads or temperatures are sensed, and provides the host system with warning of an impending shutdown, to enable it to perform housekeeping before power is lost.

Finally, it is important to check the ability of the supply to handle line transients. All supplies can do this to some extent—there is an IEC transient-test waveform, of course. But your application may see transients that are greater than that, due to nasty nearby loads (relays, motors), lightning, and other factors. You may want to add additional transient protection via a low-cost passive component on the AC mains, ahead of the supply's input.

Conclusion
Today's AC/DC supplies are remarkably efficient, compact, versatile, and rugged, while incorporating complex control strategies, algorithms and protection. At the same time, they meet a wide variety of performance and safety standards. First decide what supplies are needed and where—both functionally and physically—it will be possible to take the next step of finding a vendor and specific models that meet the project's needs and cost targets.

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Next-generation SJ MOSFETs extend performance of silicon-based power devices

MOSFET selection hinges on factors specific to the device, the circuit, and the system design

By: Franz Stückler, Infineon Technologies

For more than a decade, development of Infineon's CoolMOS™ super-junction (SJ) MOSFET technology has extended the "silicon limit line" that restricts the performance of planar-type power MOSFETs. The steady advance is a result of continuing refinement of both transistor architecture and manufacturing process to balance area-specific conduction and switching losses. The latest CoolMOS C7 MOSFETs set new levels of performance for design of the highest-efficiency power supply and power conversion systems.

Since the first commercial launch of CoolMOS SJ MOSFETs in 1998, Infineon has introduced two device families targeted at specific markets and several others intended for broad application in power switching. CoolMOS C7 is the latest technology for Best-in-Class performance in Power Factor Correction (PFC) and other hard switching topologies. It provides a significant reduction in device size and higher application performance than previous families. Comparison of several devices [**Figure 1**] illustrates how super-junction devices in general have re-defined the silicon limit line, and shows how the C7 series achieves area specific $R_{DS(on)}$ of less than 1 Ohm*mm². With corresponding major reductions in device capacitances, all important Figure of Merit (FOM) indicators of C7 are incredibly low.

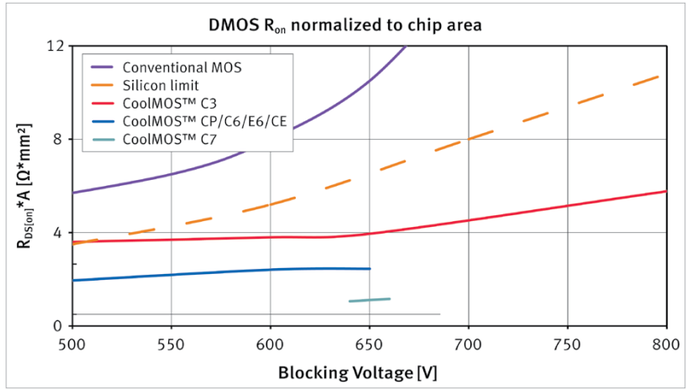

Figure 1

To best leverage the outstanding performance characteristics of C7, power conversion designs need to account for the specific behaviors inherent to the technology. This article examines both the general behavior of SJ MOSFET devices and specific characteristics of C7 to provide guidance in selecting the best device for a given application.

SJ MOSFET Characteristics
In conventional high-voltage planar MOSFETs, about 95% of overall blocking voltage is in the drain drift region. [**Figure 2**] The limits of this blocking voltage are a function of thickness and doping. In a SJ MOSFET, the drain drift area is heavily doped to reduce the on-state resistance. P-doped columnar structures are added, and

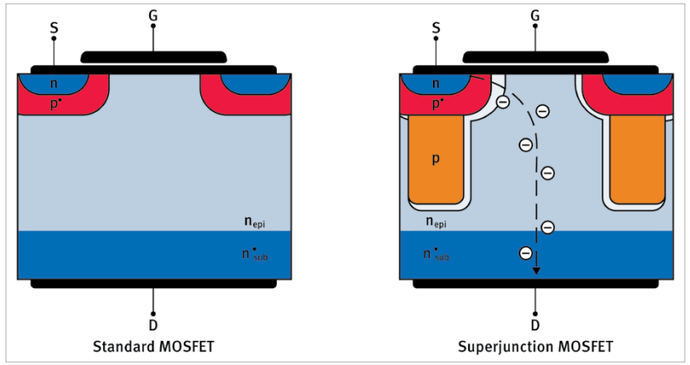

Figure 2

these columns and the n-doped regions are dimensioned to achieve high blocking voltage when the transistor is turned off.

In its first generation, the dramatic reduction in area specific resistance of a super-junction MOSFET allowed a five-fold reduction in chip area compared to standard planar devices at that time, accompanied by lower capacitance and dynamic loss figures. These characteristics have been amplified in C7. Due to its balanced device structure, this seventh-generation SJ MOSFET delivers lowest switching loss times $R_{DS(on)}$ for hard switching topologies.

The value of area-specific conduction and switching loss balance for high voltage transistors increases as designers seek higher power density through efficiency (lower losses) and higher switching frequencies (to reduce passive component size). While the balance between higher load currents, lower switching frequency and area specific loss shifts between different MOSFET technologies, better

nation of FOM improvement, very low gate charge, and low output capacitance makes it possible to switch at high voltages in just a few nanoseconds. For this reason, the **dv/dt limit of C7 has been enhanced to 100V/ns** compared to the standard 50V/ns of other SJ-MOSFET devices.

A more detailed view of the electrical characteristics of three typical CoolMOS devices illustrates the

Specification	Symbol	IPW60R041C6	IPW60R045CP	IPW65R045C7
Max on State Resistance 25°C	$R_{DS(on)}$	41mΩ	45mΩ	45mΩ
I_D Current Rating; *D=0.75	I_D	77.5A*	60A	46A
I_D Pulse Rating	$I_{D,\ pulse}$	272A	230A	212A
Area Specific R_{on} (Ω*cm²)	Ω*cm²	24mΩ*cm²	24mΩ*cm²	10mΩ*cm²
Typical Gate to Source Gate to Drain Gate Charge Total	Q_{GS} Q_{GD} Q_G	36nC 150nC 290nC	34nC 51nC 150nC	23nC 30nC 93nC
Typical C_{iss}	C_{iss}	6530pF	6800pF	4340pF
Typical C_{rss} @ 400V	C_{rss}	33pF	9.4pF	12.4pF
Typical C_{oss} @ 400V	C_{oss}	130pF	220pF	70pF
E_{oss} @ 400V	E_{oss}	22µJ	28µJ	12µJ
Typical Effective Output Capacitance Energy Related	$C_{o(er)}$	235pF	310pF	146pF

Table 1

area-specific $R_{DS(on)}$ and lower capacitance, if used properly, will deliver the lowest losses in high density power systems.

Super-junction MOSFETs also show a stronger nonlinearity of capacitance, due to the large area for the output capacitance at low voltage formed by the P-columns. As blocking voltage rises during switching, and the depletion region folded around the P-columns becomes a planar blocking region, *Coss* and *Crss* drop dramatically. This drop is even more pronounced with C7 CoolMO transistors and contributes to low switching losses, especially in hard switching applications. The combi-

advancements made in C7 [**Table 1**]. The most obvious change is the substantially improved area specific $R_{DS(on)}$ and the lower $R_{DS(on)}$ ratings now available in standard packages. Beside this obvious change the switching behavior has also changed for the much better.

Due to the comparatively lower *Coss* at high voltage and **faster switching** for the gate drive, **E*on* and E*off*** losses drop considerably for C7 compared with the C6 and CP devices. The results of Eon and Eoff characterization measurements for CoolMOS C7, CP, and C6 explain why. In tests made with 25A drain current load, V_{GS}=12V, V_{DS}=400V, and a range of gate

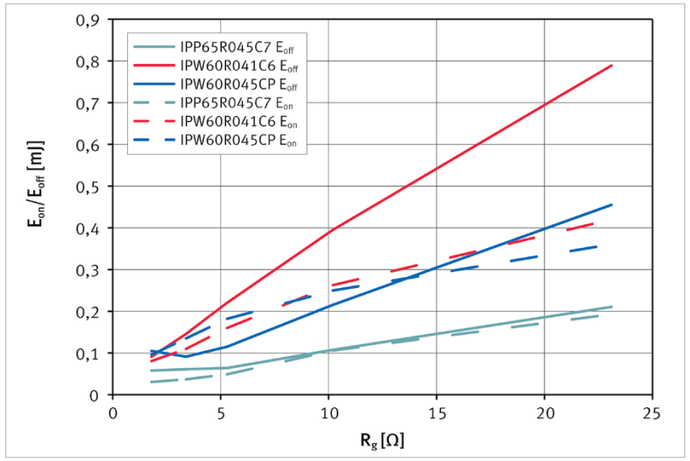

Figure 3

resistor RG from 1.8 Ohms to 23 Ohms, there is the expected range of decreasing losses as a function of lower gate resistance. Interestingly, C7 also achieves losses under 0.1 µJ with resistance levels easily 10 times higher than for C6 due to the differences in *Crss* and total *Qgd* charge. CP also requires much lower RG to get in the range of comparable turn-off loss, and cannot match the turn-on loss of C7. [**Figure 3**]

Dynamic Switching Application Considerations

With the speed of C7, secondary effects such as package inductance and PCB parasitic inductance have increased impact on switching behavior. Turn-on behavior in particular is strongly influenced by the overall application circuit and associated components. Interestingly, turn-off behavior continues to be dominated by MOSFET characteristics, i.e., the interaction of internal and external gate resistance and capacitances. A

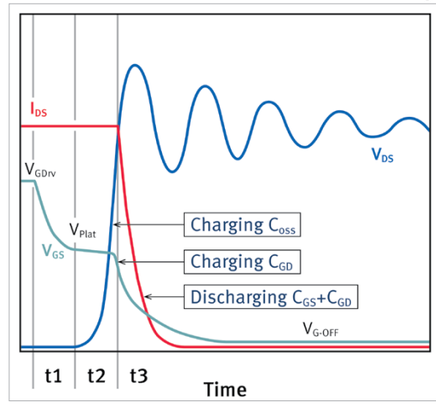

Figure 4

simulation of turn-off behavior [**Figure 4**] displaying the gate input waveform, drain to source voltage, and drain current shows how the gate drive retains complete control over the dv/dt of the MOSFET, and is directly sizable by adjusting the size of the gate input resistor. However, as gate charge and *Crss* at high voltage become lower in MOSFETs and output capacitance non-linearity increases, using low values of gate drive resistance eventually shifts the switch-off behavior into a different mode.

With very low values of gate driver resistance, di/dt is more under control of the surrounding circuit elements of the MOSFET [**Figure 5**]. For example, with a gate input resistor of 1.8 Ω for an IPP65R045C7, di/dt rises quite rapidly with load current, until limited by external parasitic inductance. In this case di/dt quickly reaches thousands of amperes per microsecond. With the gate resistor raised to 5-10Ω, the situation moderates, and the rate of charging Cgs controls the di/dt independently of drain circuit loading, keeping peak di/dt in this case to a fast 2,000 - 3,000A/µsec.

Under conditions in which the gate drive turn-off is very fast, in combination with a relatively high *Coss*, and drain to source voltage is below 50-60V, the switching behavior will be dominated by different mechanisms. Also, the drain switching voltage will not be controlled by the gate drive current, but by Coss and load current. This mode does result in very low turn-off losses, as might be expected, but it has some characteristics that must be controlled in certain applications, such as PFC boost converters, which can see a wide range of input current and brief but high overloads. A comparison of several device choices for a typical PFC design **[Table 1]** shows that it will be worthwhile to work though these issues to use the C7 technology, particu-

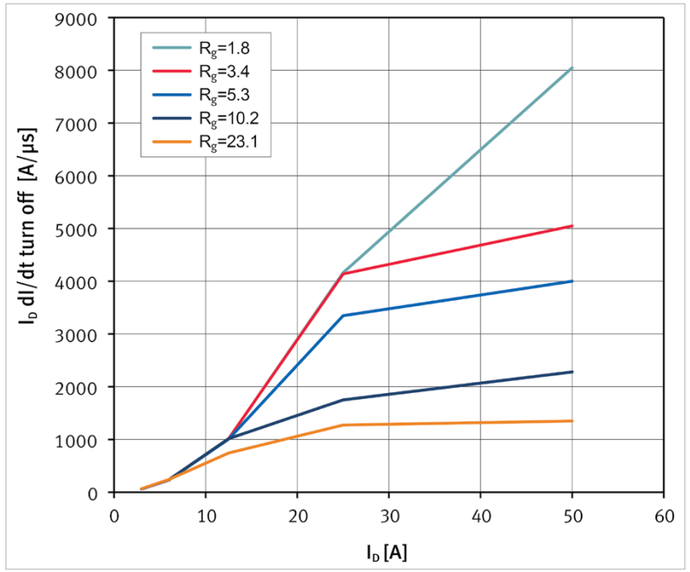

Figure 5

larly if light load efficiency and low gate drive power are considerations, or using a smaller package with lower inductance like the TO-220 (IPP65R045C7) will benefit the design.

Figure 6 compares efficiency in PFC between the IPW60R045CP, the IPW60R041C6 and the IPP65R045C7, showing the efficiency differences normalized to that of the IPW60R045CP. The maximum output power of 2500W in this graph refers to the range where this class of MOSFET is used (typically 1800-2400W), and this plot would typically reveal differences in the area of efficiency peaking for the PFC converter at half power.

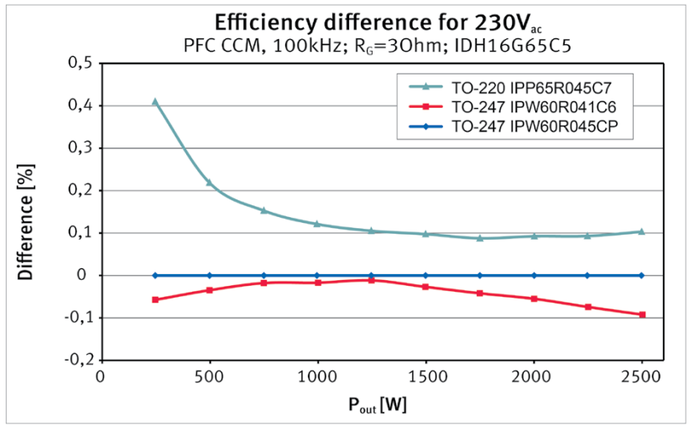

Figure 6

Looking at the comparison of CP and C6, the differences arising from FOM ($R_{DS(on)}$*Q_G and $R_{DS(on)}$*E_{oss}) and switching loss approach a breakeven point at 1200W. At this power and output current, the FOM advantage of the IPW60R041C6 is swamped out by the lower switching losses for high current of the IPW60R045CP.

Examining the IPP65R045C7 in comparison, a marked advantage in light load efficiency is seen due to the much lower *Eoss* loss and the generally better dynamic properties. At 1800W, it also maintains an advantage over both CP and C6. Although the temperature and therefore also the $R_{DS(on)}$ is increased for TO220 at 2500W, the IPP65R045C7 maintains efficiency due to the very low switching losses of C7-Technology. This effect is understandable, as the C7-Technology has much lower switching losses for same $R_{DS(on)}$, as shown in **Figure 3**. Therefore C7 is the enabler for increasing the frequencies without losing efficiency in the application.

In the end, the optimum MOSFET selection for a specific application hinges on evaluation of factors specific both to the device and to the complete circuit and system design. With the launch of devices such as the CoolMOS C7 family, designers have greater flexibility to achieve the right balance of size and system efficiency.

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Peak efficiency figures are little more than marketing hype

Figures are sometimes cherry-picked to shed the best possible light

By: Jeff Schnabel, CUI

It is a well-known fact that engineers do not appreciate being advertised to. In my experience, they tend to prize function over style and want accurate information without attempts to massage the data. This is why the all-mighty datasheet continues to be the primary-source of technical information engineers turn to when evaluating components for their design.

But here, as in advertising, figures are sometimes cherry-picked to shed the best possible light on a particular component. This practice is done throughout the electronics industry and, in our industry - power supplies – this comes in the form of efficiency figures, typically quoted as the highest point along the efficiency curve of a particular device.

When peak efficiency is used as a determining factor to select a power supply for a particular application, the design engineer must dig deeper to understand the test conditions used to derive this number; line, load, temperature, and airflow can all affect the stated efficiency. For example, an ac-dc power supply's efficiency quoted at 230 Vac line voltage may actually operate at levels 6~10% lower if run at 120 Vac. As another example, when a power supply is tested for efficiency immediately at start-up, the number will appear higher than when measured after the unit has reached thermal equilibrium, which in reality is much closer to real world conditions.

In short, peak efficiency data can provide a decent snapshot of how the power supply will perform within an application, but it does not paint the entire picture. Systems run in a variety of modes of operation and the power supply needs to be able to operate efficiently and effectively over the application's complete range of loading conditions.

Because of this, OEMs also need to seriously consider the entire efficiency curve, as well as the no-load power draw of the supply.

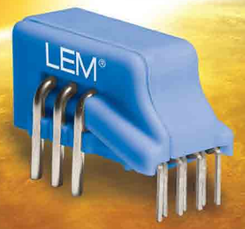
Today power supplies from the majority of vendors deliver peak efficiency percentages in the low-to-mid nineties. While this performance is certainly impressive, many applications will not operate at the power supply's efficiency "sweet spot" the majority of the time. If the power supply is not optimized to address this type of loading profile, overall efficiency will be well below the peak figure, making the touted peak power figure little more than marketing hype.

Standby power

As existing power topologies begin to reach their limit with regards to operating efficiency improvements, a new battle line is being drawn in the quest to reduce overall power consumption.

It is estimated that anywhere from 5-10% of the total power consumed in the United States is through 'vampire draw', power lost while electronic equipment is in standby or sleep mode. Governments have already identified that this is a major problem in external power adapters. Agencies such as the California Energy Commission (CEC) and the European Union through their EuP directive have put measures in place to set limits on the standby power consumption in all external ac-dc adapters shipped into their jurisdiction. The strictest standard,

Dawn of a new intelligence for current measurement



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currently classified as Level V, sets the no-load limit at 0.3 W for power supplies rated under 50 W and 0.5 W for power supplies rated between 50 and 250 W.

Although standby power consumption regulations do not currently exist for most internal ac-dc power supplies, greater attention is now being paid to this measure in the end equipment that incorporate these modules. CUI have been working to address this trend, most recently in the medical and home healthcare industry. The medical electronics market, currently estimated to be $150 billion in size, is expected to grow at a 9% rate or the next 5 years. As new medical equipment proliferates into the market, greater attention will be paid by customers and regulators to the energy consumption of these designs. In response to this trend, CUI has recently released a line of open frame ac-dc medical power supplies that not only provide operating efficiencies over 91%, but also offer standby power levels as low as 0.3 W. The VMS series is available in power levels of 20, 40, 60, and 100 W, and housed in compact open frame packages.

Flattening the curve

It's clear to many within the industry that simply driving towards higher peak efficiencies in power supplies in not the right answer, and in order to achieve greater real-world efficiencies, we need to flatten a supply's efficiency curve.

We're never going to reach a situation where a supply delivers 100% efficiency across the curve, but power supply manufacturers throughout the world are looking fervently for ways to create a device with the peak maximized across a significantly broader range of the spectrum.

Here at CUI, we're applying greater levels of intelligence to achieve this. For example, our NEB series and NQB series intermediate bus dc-dc converters incorporate a 32-bit ARM-based microcontroller running power-optimizing firmware. This provides peak performance across a much wider range of loading conditions when compared with the vast majority of competing devices currently on the market. The efficiency curves below highlight the NQB series next to a more conventional dc-dc converter. The NQB series exhibits a very flat curve from 20% all the way to 100% load, maintaining performance close to peak efficiency throughout this range.

Conclusion

Efficiency is an essential metric when choosing a power supply, but engineers need to consider more than just the peak figures and instead examine the complete curve in relation to their line and load profile to truly improve the power efficiency performance of their designs.

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Maximising the value in modern Power System designs

The issue of the power source is nearly always left until the last minute

By: Rob Hill, Powerstax

In what can be an increasingly cutthroat business environment, the engineers of original equipment manufacturers (OEMs) are under huge pressure to deliver products that will differentiate themselves from those offered by rival operations. Often they need to do this within tight deadlines, so that windows of opportunity are not missed. Unfortunately, despite the fact that it is vital to the system design, and the success of the product therefore hinges upon it, the issue of the power source is nearly always left until the last minute.

In order to augment the effectiveness of the product, the conversion efficiency rates of the power source must be raised. Switching speeds also need to be increased to minimise the size of the magnetics so that the space into which the source will fit can be squeezed as much as possible. The utilisation of standard off-the-shelf power supplies is unlikely to be particularly attractive in such circumstances due to their generic nature. Though these items are easily accessible and reasonably priced, they will bring performance penalties, as voltages will not be optimised, resulting in lower degrees of conversion efficiency for a given application. This will not only increase the overall power budget, but will also mean there is a greater quantity of heat to be dissipated - potentially shortening the operational lifespan of the product.

Though the implementation of a fully customised power solution will provide OEM engineering teams with exactly what they need performance-wise for their new products, and do so at the optimum price points for guaranteed high unit volume projects, this is rarely the situation that we see in the real world. Normally, any prediction on the actual quantities to expect will not be defined that well - in fact it is more likely that it will be nothing more than the result of optimistic guesswork conjured up by the marketing department. Though the commercial element of an OEM can, to some extent, afford to be bold about the predictions it makes, the engineering department cannot take that gamble. They need to base their judgment on something that is far more tangible, as key decisions about how the design and manufacture is undertaken will be made on this - with the costs associated with these decisions proving crucial to the end products commercial viability. If volume shipments are assured, then opting for a full custom approach is clearly valid. For example, when producing consumer devices like flat panel TVs, the volumes are expected to be high from the start, so every dimension of the development and manufacturing is geared towards highly optimised custom designed component parts that will augment system performance and lower the end product's unit cost - normally through large upfront investment. However, in most cases OEMs really need to test the market, before committing to this - as the heavy non-recurring engineering (NRE) costs initially involved will only be justified if the volume targets are met. Otherwise the revenue generated from sales will simply not be enough to cover the capital that has been ploughed into the project.

As well as the cost considerations there are other drawbacks that should be taken into account before embarking on creation of a full custom power system. Often these

Figure 1: CAD drawing & photo of completed semi-custom design for a high-rel radar implementation within a space constrained enclosure

systems will rely on unproven technology. This heightens the risk involved and can lead to delays in the end product's release plus unforeseen costs being accrued, as reworking of the design is done.

The Middle Way

Not wishing to be bound to potentially crippling NRE costs and keen to avoid being left exposed to the possibility that redesign work may need to be carried out, OEMs are now looking for another way of getting the power source they want. A way that combines the plus points of the custom and off-the-shelf approaches previously detailed. Following a semi-custom strategy presents engineers with a method by which to gain marked performance advantages over standard power sources, while simultaneously mitigating both the upfront costs and the risks that are characterised by full custom power designs.

Though they have to accept that there may be some downstream costs or reduction in profit margins if large quantities are actually achieved, this is far less likely to impact on their business than the full custom alternative would if volumes failed to materialise. Furthermore, following strategy still leaves a migration route open once the market demand necessary to support a full custom design has been proven to exist.

Because the power system is generally, as already pointed out, the last thing that gets attention in the product development process, the time pressures here are at their most pronounced. By basing the power system design on the use of ready-made, high density building blocks through which a semi-custom solution can be created time can be saved. Each block will already have all the necessary approvals (CE, UL, etc.), so the approval process for the end product will be quicker and cheaper to carry out than a full custom, where approval would effectively need to be done from scratch and often proves to be a long drawn out affair. (**See Figure 1**.)

As everything else within the design will have already been taken care of, the space that is left for it may well be difficult to utilise. This is why engaging with a company which is highly experienced in both the mechanical and thermal management aspects of power system design will pay dividends.

In conclusion, working with a power supply vendor on a full custom solution that the desired performance targets and low units costs can be reached is not as easy as it first appears. In many cases the time and initial expense involved will outweigh the actual benefits, especially if there is any doubt about the volumes that are likely to be called for. With cash-strapped OEMs looking to avoid heavy capital investment, semi-custom solutions are far better suited to addressing markets where there is still some uncertainty on how much business is likely to be generated. By utilising a modular approach, based on innovative, industry-proven brick technology and power engineering expertise, certain power source suppliers can now enable performance levels approaching those associated with custom designs to be realised without the hazards of large upfront expense, a lengthy development period or technical problems arising. Time-to-market can be shortened and the dent in the OEM's financial resources lowered considerably.

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New power architecture addresses PFC load efficiency issues

Compound Power Converter architecture promises flexible, efficient power factor correction

By: Thomas Lawson, Cognipower

As Power Factor Correction (PFC) migrates to lower power AC/DC converters, maintaining efficiency at low loads becomes an increasing challenge. The approach usually taken involves adding an extra boost conversion stage feeding a second buck conversion stage. The boost stage performs PFC at the input while the buck stage performs regulation at the output. An active bridge front end, sometimes called a "Bridgeless" system, is a more efficient variant on this approach, because one series diode is eliminated from the input path.

The PFC boost stage produces a relatively high DC voltage, which is stored in a bulk capacitor. The stored voltage serves as the input for a subsequent down-regulation stage. All the power moves through both stages of power conversion in series. Therefore, the efficiencies of the two stages multiply, i.e. 90% * 90% = 81%. The two-stage approach does not take full advantage of the flexibility implicit in a bridgeless input stage.

Compound Converter architecture

PFC and regulation functions are blended together for better efficiency in CogniPower's approach to address the issue, Compound Converter architecture. The key difference in a Compound Converter is the optimization of the placement and use of the storage element. The storage could be moved to the output, by providing extra capacitance at the output filter, but the result would be to maximize the amount of capacitance required for good regulation. That would also maximize the size and cost of the filtration. A more efficient approach is to provide separate storage to support the output during the zero crossing periods of the AC input, but not to route all the power that is converted into, and out of, the storage element.

The two stages in a Compound Converter operate in parallel, not in series. The result is that the majority of power moves through a single stage of power conversion. That difference enables a substantial efficiency gain. When a PFC boost conversion stage is running with a near constant ON time, the Power Factor will be near ideal. At a particular fixed ON time, the correct amount of power will be transferred from input to output during each single AC cycle. However, during parts of the cycle, there will be excess energy available, and during other parts, there will be a deficit of available energy.

In a compound converter, the storage capacitor both accepts the surplus and provides the shortfall, as appropriate, but is not involved with the transfer of the majority of energy from input to output. During periods of sufficient AC energy availability, the load is serviced directly, with any excess energy going into storage. At times in the AC cycle when not enough energy is available to supply the load, supplemental energy is provided from storage. In that fashion, most of the energy transferred can move from input to output through only a single stage of power conversion. Efficiency rises.

The storage voltage varies at twice the frequency of the AC line, and is regulated only on the

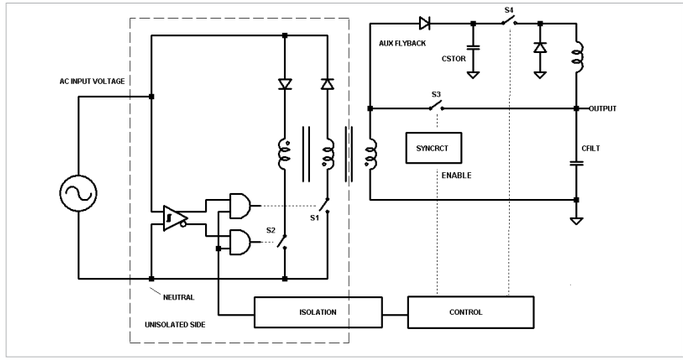

Figure 1: Block Diagram of an Isolated AC/DC Compound Converter

average. The loop that controls the storage voltage should be slow compared to the line frequency to obtain the best PFC behavior. Because the storage voltage can vary over a wide range, a much smaller capacitance is required to support a given load than when the capacitance is placed at the output. Also, the storage voltage can be lower, eliminating the need for an expensive, high-voltage capacitor for storage.

In a Compound Converter, 2/3s of the power might move through a single stage at 90% efficiency, and 1/3 might move through both stages at 81% efficiency, for an overall efficiency increase from 81% to 87%. When the output voltage is allowed to droop a little more during supplemental converter operation, even higher efficiencies gains can be achieved. In addition, all the usual steps known to further increase the basic efficiency of either the main or supplemental stage can be applied here, as well.

Because a larger percentage of the power moves through only a single stage of power conversion at lighter loads, Compound Converter architecture makes it easier to meet efficiency standards at light loads. There are advantages when heavily loaded, also. In a conventional two-stage converter, both power stages must be built to withstand the maximum power levels. In a compound converter, the main and supplemental stages share the maximum load. The main power path can be optimized for efficiency at average power levels, while the supplemental path can supply surge currents to satisfy transient loads, improving both efficiency and regulation.

The hardware and control requirements to create such a system are surprisingly simple. The component count can actually drop in comparison to the normal two-stage approach. Regulation in a compound converter is better because of the presence of a local, supplemental supply of energy at a convenient voltage. The supplemental conversion stage can run at a higher frequency than the main converter for even better regulation and lower output ripple.

Wide application area

Compound architecture can be applied to a wide variety of converter topologies including forward converters, zero voltage switching converters, DC to DC, AC to AC, multiple output converters, and even power amplifiers.

Figure 1 shows a Compound Converter in block form. The left-hand, AC-side of the figure is a bridgeless boost stage acting on the dual primaries of the transformer. Alternatively, a single-primary transformer could do the same job if connected in a full bridge. The topology shown in **Figure 1** minimizes the number of series diodes or switches at the expense of an additional transformer winding.

The AC-side switch intelligence is located on the right-hand, isolated side. A single bit of data representing ON or OFF is sent across a simple digital isolation barrier. Switch 1 or 2 energizes one of the transformer windings based on the polarity of the AC input voltage. Switch 3, operating as a synchronous rectifier, completes the main flyback function.

With the addition of a control input to disable Switch 3, that switch does more than just synchronously rectify the main flyback stage. It also provides local regulation. Switch 3 is opened when the load is satisfied, allowing surplus

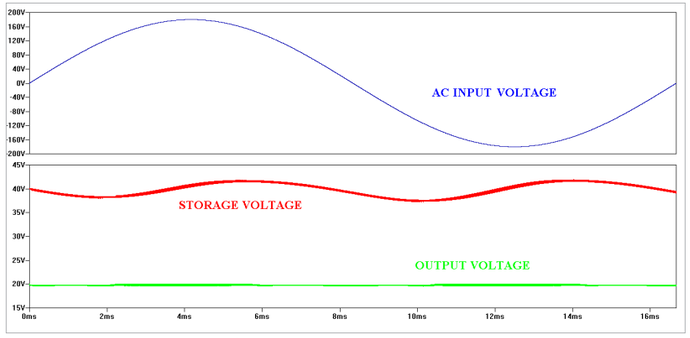

Figure 2: SPICE Output Showing Output and Storage Voltages

inductive energy to be transferred to the storage capacitor through the auxiliary flyback diode.

The remaining circuitry is an auxiliary buck converter to move energy from the storage capacitor to the output. The auxiliary control circuitry will cause the supplemental converter to support the load during zero crossing, or during interruptions in the AC input. If the supplemental converter regulates to a slightly lower voltage, it will only act after the main regulator begins to drop out. That effect increases efficiency. The lower the load presented, the greater the improvement in efficiency. The supplemental regulator can operate out of phase with the main regulator to reduce ripple. If at any time a transient load should disturb the output, the supplementary converter can act immediately to help restore regulation, reducing the peak requirements for the main stage.

Control is simpler than one might think

The main converter can operate in discontinuous or continuous mode. The basic controls involve three simple loops.

Loop 1, Synchronous rectifier: Switch 3 closed if the load requires energy when inductive current would flow in the desired direction.

Loop 2, Supplemental buck: Close Switch 4 whenever the output is below the supplemental reference voltage

Loop 3, Constant ON time for transformer primary switches: Heavily filtered slow loop to keep the storage voltage within broad limits. The constant ON time will not change significantly during a single AC cycle. A maximum ON time prevents excess current from flowing during transients or during start-up.

Figure 2 shows a simulation of a 100 Watt Compound Converter running from 120 VAC at 60 Hertz. The output is here 20 VDC, though a wide range of output voltages is practical. The storage voltage varies at twice the line frequency. In this case, the nominal storage voltage is 40 volts. Higher storage voltages increase the holdover time for a given value storage capacitance, but require higher voltage components. The minimum storage capacity should support the maximum load during one AC zero crossing. More storage will support a missing AC cycle, or longer periods of AC drop-out. With substantial storage available, the Compound Converter becomes a Uninterruptible Power Supply.

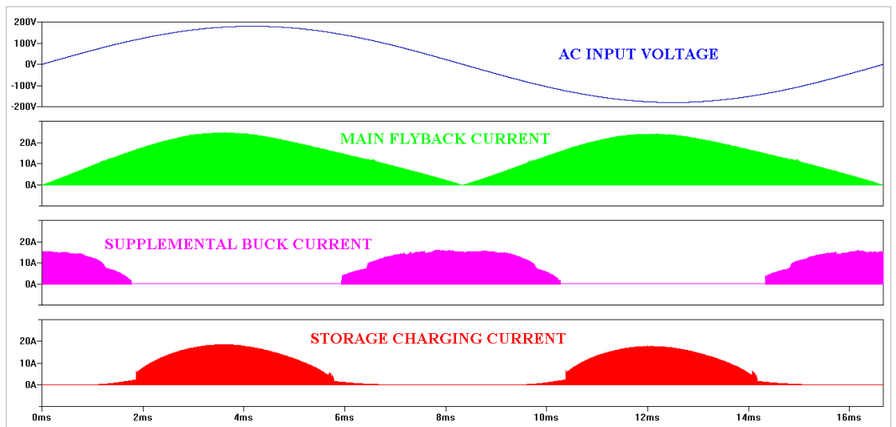

Figure 2: SPICE Output Showing Output and Storage Voltages

Figure 3 shows simulations of the converter running at 50% load. The top trace is a single cycle of the AC line voltage. The second trace shows the current supplied to the load through the main flyback path. The third trace shows the current supplied to the load through the supplemental buck path. The bottom trace shows current flowing into the storage capacitor during the period of excess energy availability. Note that on average, the power going into storage will nearly equal the power being supplied by the supplemental buck converter.

Other Considerations

Because control of the switches on the AC side is provided by circuitry on the DC side, a chicken-and-egg situation must be avoided at start-up. There are several ways to handle that issue. One is to add a separate, bootstrap, self-oscillating supply that has two secondary windings. One winding provides power for efficient switch drive on the AC side, the other powers the Control block on the DC side. CogniPower has a simple, efficient design for such a bootstrap supply. Another possibility is to add start-up circuitry on the AC side which operates only briefly, and without feedback when power comes up, to move enough energy through the transformer to allow the Control block to begin to function.

As with other types of power converters, further light load efficiency gains can be achieved by reducing the underlying frequency of operation. When synchronous behavior is not required, regulation and good PFC can also be achieved with a completely fixed ON time and a slowly changing frequency of operation.

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High-power controller handles LEDs, solar cells, batteries, and other demanding consumer apps

Device steps down 60V inputs, can reduce BOM costs, and improve reliability

By: Luke Milner, Design Engineer, Linear Technology

The best LED drivers accurately regulate LED current for consistent color reproduction and modulate it rapidly for high contrast dimming. They also recognize and survive short and open circuits, monitor and report current levels, guard against overheating, and protect weak power supplies from excessive load currents. A standard switching converter would require a number of additional expensive amplifiers, references and passive components to fulfill these responsibilities.

In contrast, the LT3763 LED driver-controller has these functions built in—reducing BOM costs, saving board space and improving reliability. The LT3763 is more than just a high performance LED driver. Its rich feature set simplifies the design of other demanding applications, such as safe charging of a sealed lead-acid batteries, or maximum power point regulation for a solar panel, or a combination of both. The LT3763 performs these tasks with high efficiency, even at input voltages reaching 60V.

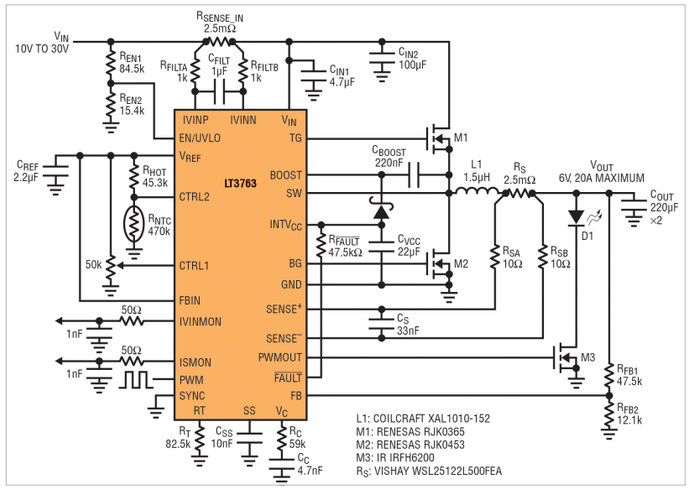

Figure 1: A single high power LED (20A) driver with analog and PWM dimming

Driving LEDs

Figure 1 shows the LT3763 configured as a high power LED driver. A potentiometer at the CTRL1 pin permits manual adjustment of the regulated LED current from 0 to 20A. For thermal regulation of the LED current, a resistor with a negative temperature coefficient is mounted near the LED and connected from the CTRL2 pin to GND.

The resistor network at the EN/UVLO pin programs the LT3763 to shut down if the input voltage falls to less than 10V. The resistor network at the FB pin defines an open-circuit condition as when the output reaches 6V, and should that ever happen, the LT3763 automatically reduces the inductor current to prevent overshoot and pulls down the /FAULT pin to mark

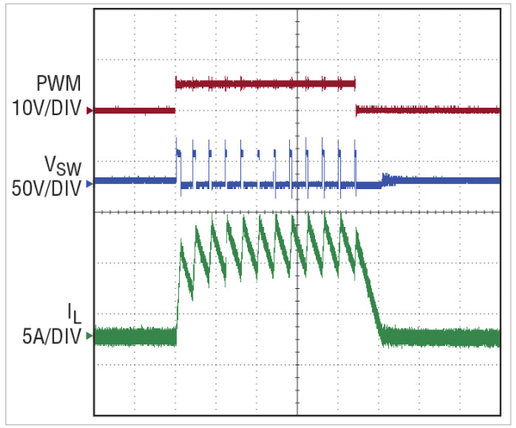

Figure 2: PWM dimming performance of the circuit in Figure 1

the occasion.

The LT3763 is designed to provide flicker-free LED dimming as shown in **Figure 2**. This is achieved by pulling PWMOUT low whenever PWM is low and thereby disconnecting the LED, by similarly disconnecting the compensation network at VC, and resynchronizing internal switching clocks to the PWM pulse. These maneuvers ensure that subsequent pulses are identical, that the inductor current rises as fast as possible to satisfy the programmed LED current level, and that the LED light never flickers.

The LT3763 can be configured as in **Figure 3** to deliver 350W with 98% efficiency from a 48V input. An internal regulator supplies the drivers of the TG and BG pins with enough power for each to drive two of the external NMOS power switches. Higher power applications can be built by connecting LT3763s in parallel, so that current is shared equally between the two controllers. This configuration also illustrates how the SYNC pin can be used to synchronize the parallel connected LT3763s to an external clock.

The high output voltage rating of the LT3763 enables 35V at the output with the simplicity of a standard buck converter. The output voltage can be as high as 1.5V less than input voltage, and the configuration in **Figure 4** makes use of this feature to charge three sealed lead-acid batteries in series (up to 45V) from a 48V supply.

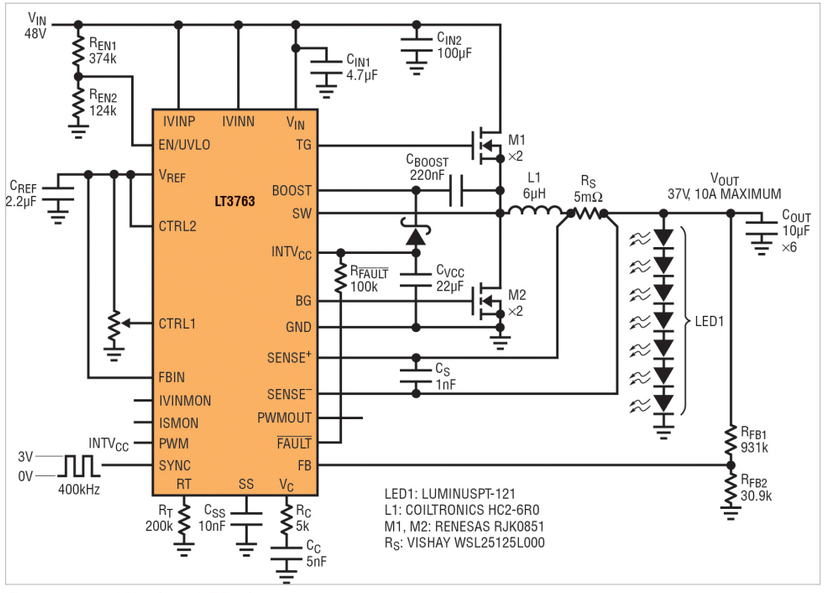

Figure 3: 350W white LED driver

Charging batteries

The battery charger shown in **Figure 4**, like all chargers, must be able to precisely regulate the batteries' rated charging current (constant current mode) until the battery voltages reach the limit set by their chemistry. The charger must maintain that voltage (constant voltage mode) without overshoot until the current drawn by the

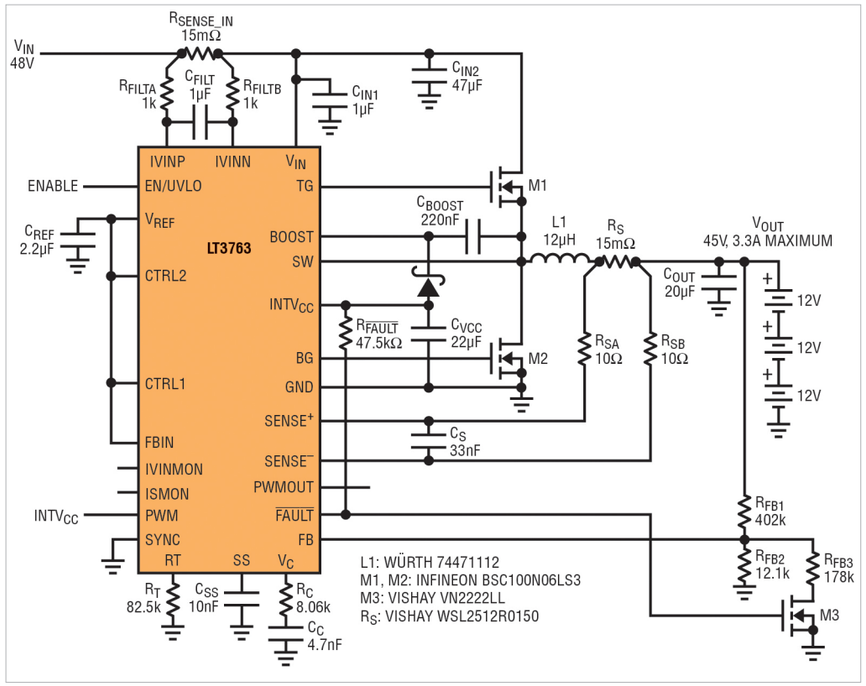

Figure 4: 3.3A, six-cell (36V) SLA battery charger

trickle-charging batteries becomes very small. Once the trickle charge phase is complete, the charger should allow the batteries' voltages to decay to a relaxed level before finally settling at and holding that final voltage indefinitely.

The combined current and voltage regulation loops on the LT3763, and its LED fault handling circuitry, nearly make it a complete battery charger. Only a single additional transistor is required to form a complete battery charging system. The resistor divider at the FB pin has been designed to program the charging voltage to 45V. As in the case of an open-circuit, when the voltage reaches 45V, the LT3763 automatically reduces the current

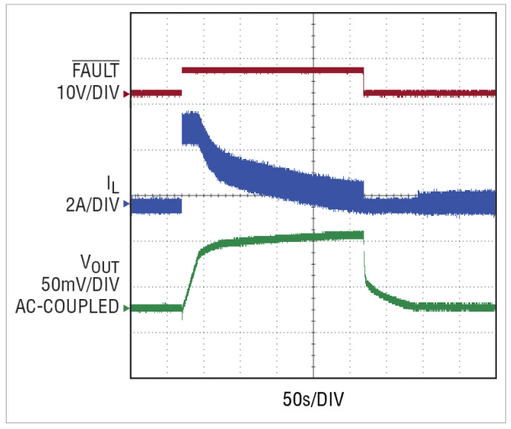

Figure 5: 36V SLA battery charging cycle

charging current reduces to ten percent of the regulated current (C/10 battery specification), the LT3763's open-circuit fault condition is triggered. The resulting high-to-low transition at the /FAULT pin is used to turn off the gate of the added transistor M3 and remove the resistor RFB3 from the feedback network. The programmed output voltage is thereby lowered, and the LT3763 stops switching to allow the batteries to relax on their own.

When their combined voltage decays to the newly programmed value, the LT3763 begins switching again and provides a sustaining current necessary to maintain the output voltage indefinitely. As an added benefit, the /FAULT pin transition serves as a signal that the trickle charging has begun.

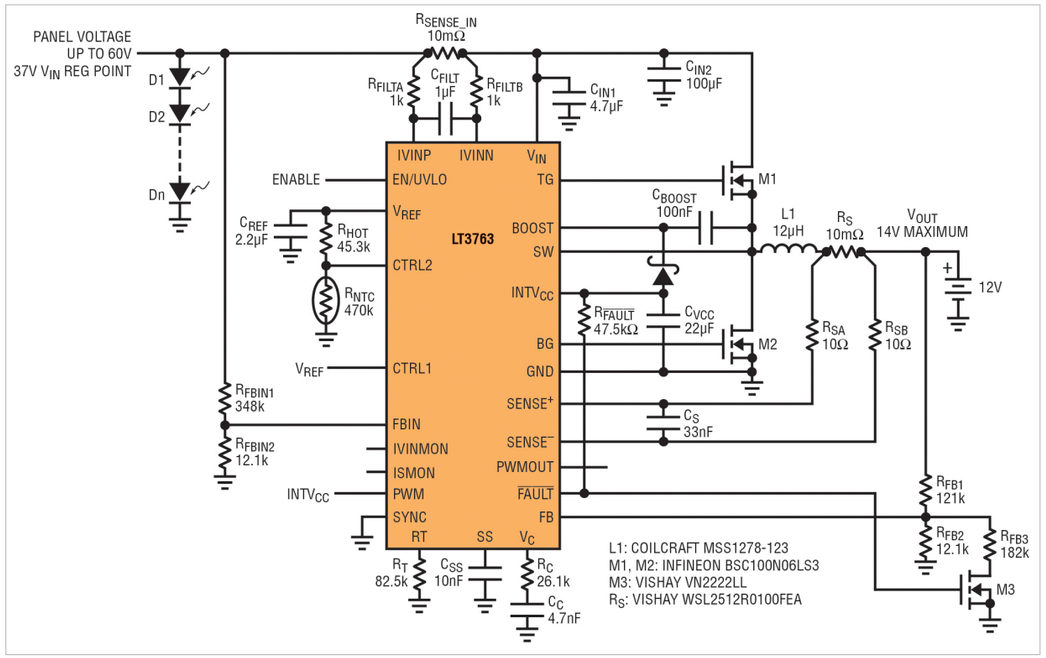

Figure 6: 70W solar energy harvester with maximum power point regulation

Regulating solar panels

a well-designed solar panel power supply requires an intelligent combination of current and voltage regulation. In an optimum design, a converter must sense the voltage on the panel and adjust the current it draws to maintain the input voltage at the panel's maximum power point. If it draws too much current, the voltage of the high impedance panel will collapse. If it draws too little current, available light energy is essentially wasted.

In many common solutions, a solar panel controller designer would use an amplifier to sense the input voltage and adjust the voltage on the current control pin. The LT3763 includes this function at the FBIN pin. Simply tie CTRL1 high, to the 2V reference available at VREF, and add a voltage divider from VIN to FBIN. When the voltage at FBIN falls to nearly 1.205V, the internal amplifier automatically overrides the CTRL1 voltage and reduces the load current. This regulates the input voltage (the voltage of the solar panel) at the maximum power point for the panel. The resistor divider on the FBIN pin is shown in Figure 6 and can be customized to fit the requirements of any solar panel.

In the configuration shown in **Figure 6**, the converter can generate whatever inductor current, up to 5A, is required to hold the panel voltage at 37V. Input voltage feedback is via the voltage divider at the FBIN pin, which in turn regulates the inductor current to what is actually necessary to hold the panel at peak power in any given light condition.

As shown in **Figure 7**, the process of charging a battery with a solar panel looks very similar to charging with a low impedance supply as before. The difference is that the regulated inductor current (charge current) is not preset by the designer, but is instead adjusted on the fly via the feedback loop regulating input voltage. This effectively minimizes charge time, since input power is maximized at

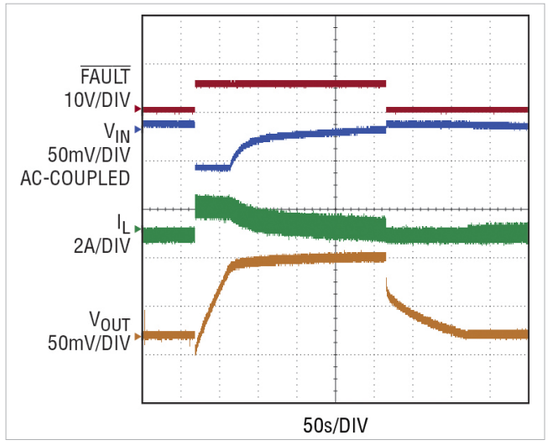

Figure 7: Solar powered SLA battery charging

all times, regardless of panel illumination. Since the LT3763 has the capability of regulating input voltage and current, as well as output voltage and current, and provides a fault flag with C/10, it can easily be used with a wide variety of solar panels to charge many different types of batteries.

Monitoring current levels

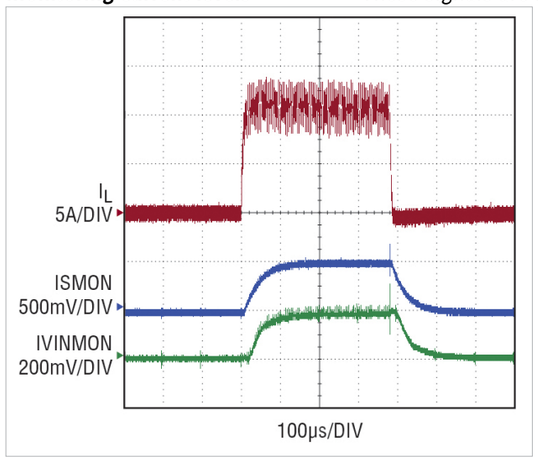

Figure 8: Current monitor outputs in an LED driver application with PWM dimming

In each of the applications presented here, the LT3763 provides an additional service by monitoring the input and output current levels. Voltages across the IVINP and IVINN pins ranging from 0 to 50mV are amplified with a gain of 20, and the resulting voltage appears at the IVINMON pin. The voltage at the ISMON pin is an identical amplification of the voltage across the SENSE+ and SENSE– pins, as shown in **Figure 8**.

These signals are helpful in systems that must verify the current provided to LEDs or measure the efficiency of voltage conversion. They can also help to estimate the power provided by a solar panel or to monitor the current trickling into a charging battery as it decays to zero.

Due to the discontinuous input current of a step-down buck converter, a low-pass filter is typically necessary at the IVINP and IVINN pins as shown in Figure 1 and Figure 4. A much smaller filter at the SENSE+ and SENSE– pins may also be useful in filtering high frequency noise, but it is not necessary. Even with these filters, the monitors are fast enough to track reasonably short PWM pulses as shown in Figure 8. Nevertheless, if a designer is more concerned with average current levels than instantaneous current levels, then additional lowpass filters can be easily added to the ISMON and IVINMON pins.

Feature integration

The LT3763 is a versatile step-down buck converter that integrates many complex features essential for not only LED drivers, but solar harvesters and battery chargers as well. A PWM driver and current monitors are included with fault detection, current limiting, input and output voltage regulation. Due to its high voltage rating, all of these features can be utilized to illuminate long strings of LEDs or charge stacks of batteries. Available in a 28-lead TSSOP package, the LT3763 is a compact, complete, and efficient power system.

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Filter capacitor considerations

Efficient power conversion in consumer electronics

By: Pat Hollenbeck, AVX

Due to the constant evolution of consumer electronics, efficient power conversion is critical for reliable performance, and the filtering of output ripple is a critical factor in supplying consistent power to the load. This article provides a breakdown of filter capacitor technologies and their respective performance characteristics regarding power conversion efficiency in consumer electronics.

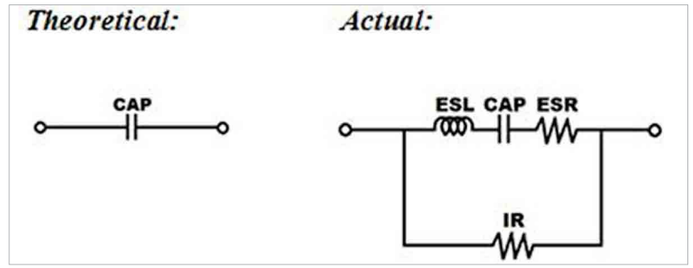

Figure 1: Theoretical (left) and Actual (right) models of a capacitor.

Continual pressure to miniaturize a system or increase its functionality means that the impact of parasitics increases in the device. In the case of an SMPS system in particular, increasing the switching frequency to improve efficiency can often result in increasing parasitic effects, each of which will then result in higher ripple voltage at frequencies in the KHz to MHz range. This ripple voltage can be greatly reduced with the correct selection of filtering capacitors in the system. Control of these parasitic effects is important to minimize heating for higher power/cc designs.

There are several characteristics of filter capacitors to consider when seeking to maximize the efficiency of power conversion systems. Ultimately, application-specific constraints will determine the ratings needed for a given system and choosing the correct technology will have a major impact on design. Certain construction, materials, and electrical properties are better suited to some applications than others, and making the appropriate selections will result in a consistent supply of power to the electronic device for its given operating conditions.

The principle drivers in selecting the correct filter capacitor are the internal parasitics associated with their materials and construction. During the selection process, consider the effects of non-ideal parasitics for a given capacitor technology. Limiting these parasitics is important to achieve power quality optimization. The three major parasitic influences on output voltage quality are Equivalent Series Resistance (ESR), Equivalent Series Inductance (ESL), and Insulation Resistance (IR).

In the actual model of a capacitor (**Figure 1**), ESR and ESL are the resistive and inductive properties of the metals incorporated into the capacitor's construction (electrodes and leads), and the IR is the resistance of the dielectric material used in the capacitor. Choosing the correct materials and proper construction techniques has a direct impact on the performance of the capacitors as ripple filters.

Typically, output filter capacitors require extremely low ESR. Low ESR values, in accordance with specific capacitance requirements, increase power quality significantly by reducing ripple voltage. A well-designed power conversion device can approach maximum efficiency (**Figure 2**).

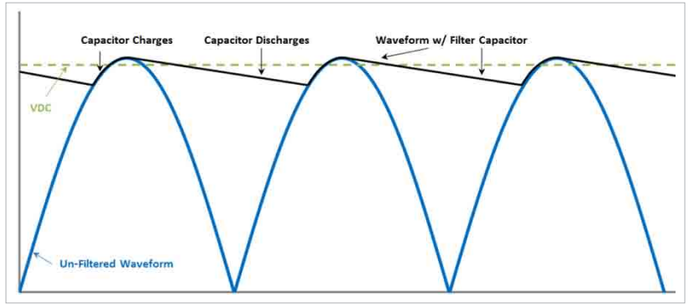

Figure 2: DC waveform filtered with an output filter capacitor. (Storr 2011)

Keeping that in mind, differing filter capacitor technologies each have their own set of advantages and disadvantages in regard to power conversion performance. Four common capacitor technology options are stacked ceramics, tantalum, film, and aluminum electrolytics.

Stacked ceramic MLCC capacitors are non-polar devices. Composed of many alternating thin ceramic layers with staggered metal electrodes, their multiple layers are stacked to increase capacitance voltage (CV) density or CV/cc per unit volume. New configurations of stacked capacitors, such as capacitors with electrodes perpendicular to the PCB traces drive, can reduce the already low ESR and ESL figures of stacked capacitors.

Plastic film, another non-polar material, can also be used as a dielectric in output filter capacitors. The term "film capacitor" defines these components, which are made of an insulating polymer film and a metal foil electrode, typically using polyester or polypropylene materials as the dielectric.

Tantalum capacitors may also be considered in these applications. Tantalum metal forms the anode, while its oxide layer makes up the dielectric. Standard tantalum technology uses manganese dioxide as the counter-electrode (cathode), as this material features self-healing properties for long life. Similarly, a polymer material can be used as the counter-electrode to achieve lower ESR values.

Aluminum electrolytic capacitors are widely used as filter capacitors in consumer applications. Constructed of an aluminum oxide dielectric, thin aluminum plates, and an ionic conducting liquid, aluminum electrolytics commonly suffer from an "end of life" wear-out mechanism due to their materials and construction.

Output filtering performance differs with each of these technologies and has a direct impact on the output voltage quality (e.g. ripple). The factors that dictate the performance of these capacitors are the previously mentioned parasitics associated with the chosen component.

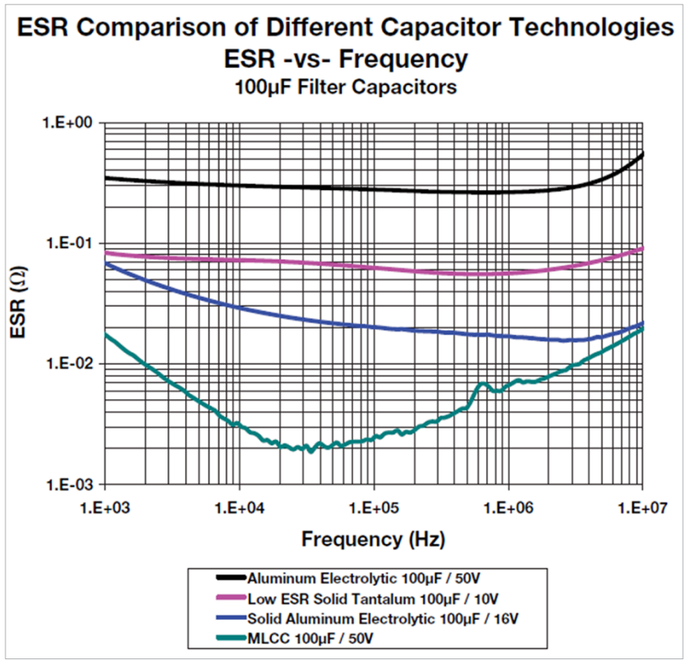

Figure 3. ESR vs. Frequency for different dielectrics

The ESR comparison in **Figure 3** demonstrates the variance in parasitic parameters for each capacitor technology over the typical operating frequency range for power conversion in consumer electronics (1KHz -10MHz).

Based on the parasitic characteristics of these technologies, it can be determined that stacked MLCC output filter capacitors exhibit significantly lower ESR values, providing more efficient filtering properties than the opposing technologies. However, in consumer electronics, board space and component costs are two additional factors that dictate device design and component selection. Since PCB real estate is at a premium in modern electronics, volumetric efficiency is critical when selecting the components utilized in the power conversion segment of the PCB.

The highest volumetric efficiency for capacitance/voltage is realized by tantalum capacitor technology. Using microchip construction methods, miniaturization of high CV components is one of the major benefits of tantalum capacitors. Ceramic chips offer footprint reduction solutions as well, and due to the significantly lower parasitics associated with the multilayer approach, smaller value MLCCs can replace larger electrical value electrolytics and tantalums. A ratio of 1:10 (ceramic to electrolytic) value is reasonable. Consequently, MLCCs offer some of the smallest-sized output capacitor options in some applications. Relative to tantalum chips, ceramic capacitors offer ESR values an order of magnitude lower for frequencies in the 10KHz range and greater. Subsequently, this leads to greater filtering efficiency in the given application in spite of the lower CV density.

For aluminum electrolytic components, parasitics are much more evident due to their rolled-foil and leaded construction approach. Their ESL and ESR values are orders of magnitude higher than those of tantalum or ceramics; thus, higher capacitance values are required to filter the voltage ripple during power conversion. In some applications where a small tantalum or ceramic could be utilized, it would require a much larger electrolytic can to be placed on the board.

Cost also plays a major role in filter capacitor selection, especially when designing high volume consumer electronics. In commercial electronics, the choice between technologies remains driven by volumetric efficiency (CV/cc), surface mount compatibility, and application ripple requirements (which, in turn, depend on the ESR and ESL ratings of the device). For power filtering, there is often an application overlap between tantalum and class II ceramic (X7R & X5R).

As these are often used in high-reliability versions of products with enhanced volumetric efficiency and minimized parasitics, their cost is typically higher. In consumer electronics, long-term reliability (e.g. 20+ years) is not as significant a factor as in military, medical, or aerospace applications. In fact, in consumer circuits, electrolytics have previously been largely unchallenged as output filters, primarily due to their low cost.

However, advances in stacked MLCC and tantalum capacitor manufacturing have greatly increased their use in a wide range of emerging consumer applications. In conclusion, electronic engineers have several options when designing filter capacitors for power conversion circuits into consumer electronics and should be sure to consider the application with regards to each devices' size, parasitic characteristics, dielectric technology, and component construction.

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MEMS Time-Keeper extends standby life of mobile devices

Battery technology has not kept up with the progress in semiconductor design

By: Jehangir Parvereshi, SiTime

With un-tethered instant access to data, news and entertainment, consumers are spending more time on Smartphones and mobile devices. Device users are demanding faster connectivity, multi-core Ghz+ application processors and HD resolution touch screens, while at the same time, expecting to last longer on a single battery charge. Mobile device designers must carefully consider how to meet the conflicting demands of extending battery life while supporting faster, more power-hungry processors and LCD screens. Design options typically fall into two main categories: 1. reduce overall power consumption, or 2. increase battery capacity.

Battery and display technologies have not kept up with the exponential progress in semiconductor design and processes over the last decade. With the space and weight constraints of MIDs, only incremental increases in battery capacity are possible using current battery technologies.

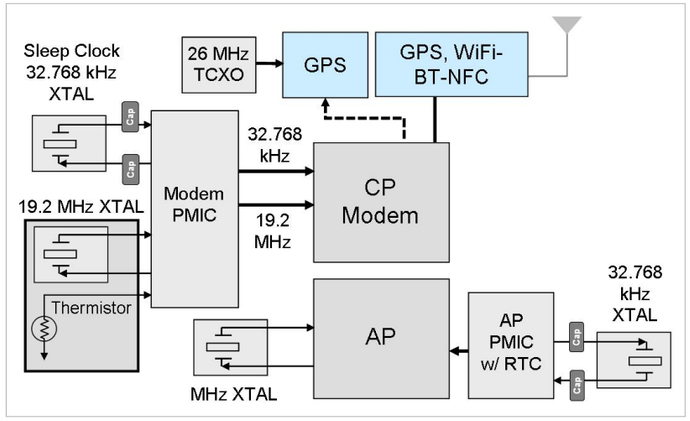

Figure 1: Block diagram showing high-level architecture of a smart phone

Designers are left to employ creative ways to reduce overall power consumption.

One technique to reduce power consumption is to shut down the functional blocks with the highest current drain and switch to the lowest power suspend/sleep state when devices are inactive. However, during the low power state, the always-ON clocks continue to draw battery power. New MEMS-based time-keeping solutions offer unique power saving strategies with programmable output frequencies and output drive swing levels. Drawing a mere 750 nA core current, these timing devices can run off of an unregulated Li-Ion or regulated power, thus bringing more options to mobile device designers.

Mobile Device Power Management Overview

The basic architecture of a mobile wireless device is shown in **Figure 1**. Depending on the implementation of the mobile device architecture, the power management function is distributed across the application and RF baseband processors and/or a dedicated PMIC (power management IC). Given their size constraints and performance

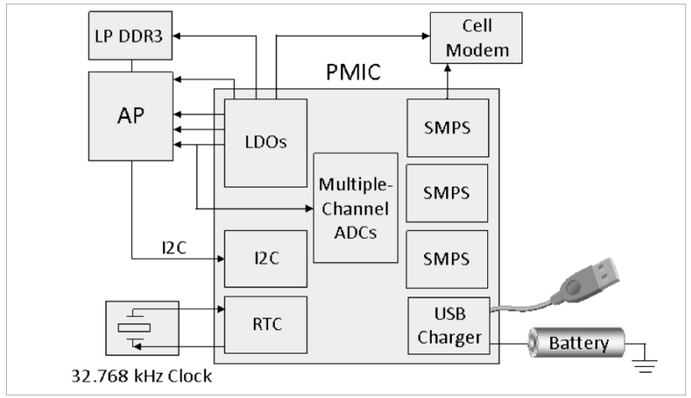

Figure-2: Functional block diagram of a PMIC

demands, these blocks are implemented in CMOS sub-micron technology.

Power dissipation in a CMOS SoC (system on chip) can be quantified by the following formula:

$P = C*V^2*F$

Where; P is the power in watts; V is the DC voltage of the individual power rail (VDD) of the SoC ; C is the intrinsic capacitance hanging off the VDD power bus. The complex blocks implemented inside each SoC are powered from multiple VDD rails ranging in values from 1.0V to 4.3V.

The basic power management function is implemented as: 1) Monitor system processing load, 2) Switch the system between one of the following states: a) Active, b) Suspend, or c) Sleep.

Active State

Power consumption can be optimized during the active state by using a technique called dynamic voltage and frequency scaling (DVFS). From equation (1), power dissipation is reduced as the square of the lower VDD rail voltage. Likewise, depending on the process node deployed in the fabrication of the SoC, the operating frequency is throttled down to linearly scale back the power dissipation.

The application processor (AP) and RF baseband processor are the main processing units and consume the highest amount of battery power. These processing SoCs achieve the highest efficiency possible by communicating commands with the PMIC or the on-chip power-management module to control the DVFS functionality. The basic functional block of a PMIC is shown in **Figure 2**. The PMIC function can be implemented as a stand-alone chip or can be distributed as embedded blocks within the processing units in a mobile phone.

The processing modules/SoCs communicate system status to the PMIC over an I2C bus or similar bus such as a SM bus. The PMIC LDO and SMPS blocks provide programmable regulated voltages required by the system power needs.

Suspend State

The suspend state is entered when a mobile device is inactive for a pre-determined (user configured) time or when initiated by the user:

- No user interface interaction with touch screen or buttons
- No incoming phone calls or data communication
- User pushed power/suspend key to force suspend state

In this state the main processing unit(s) operate at the lowest permissible VDD core voltage and clock frequency down to zero hertz. The LCD screen is shut off and the touch sensor wakes up every hundred milliseconds to detect user touch interaction. Communication peripherals such as cell modems are in their lowest power state, which can be interrupted by an external event. The PMIC running off a 32.768 kHz clock source is the only device that is fully active in this low power state. One of the functions of the 32 kHz clock is to serve as a timer to wake up the peripheral devices at pre-determined times as dictated by the wireless LAN requirements or the power management scheme.
In suspend state the system power dissipation is due to:

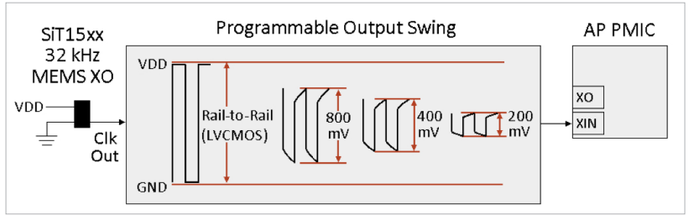

Figure 3: NanoDrive™ output swing is programmable down to 200 mV to minimize power

- Leakage current of the main processing SoCs
- Suspended state power dissipation of peripherals (touch screen, WiFi RF front-end, etc.)
- Power dissipation of the PMIC running off the 32 kHz clock

The major contributors to the overall power budget in suspend state is the power consumption of the PMIC, 32 kHz crystal oscillator, the RTC block and wireless LAN connectivity.

Sleep State

This is the lowest power state. All devices are shut down except for the monitoring circuitry clocked by the 32 kHz device in the PMIC and the real-time clock (RTC) block. To extend the standby life of the battery, creative strategies must be deployed to shave off micro-watts of power from the active blocks in the suspend and sleep states. Regardless of the power state, the 32 kHz oscillator is always ON to clock power, battery management blocks and wireless LAN. In suspend state, the current draw is typically in the micro-amps. Lithium-chemistry batteries loose more battery capacity during long periods of low-current drain typical of suspend/sleep state scenarios compared to short bursts of peak current during the active state.

Mobile Device Clocking Schemes

A typical mobile device, depending on the choice of the applications processor, partitioning and other functions it supports, can contain several timing devices including one or more 32 kHz clocks as shown in **Figure 2**. The power consumed by a 32 kHz oscillator is usually 2 to 3 micro-watts with a typical current draw of 1 to 2 uA from a 3V DC regulated power supply. The power consumed by the 32 kHz oscillator circuit, whether it is part of the PMIC crystal oscillator or an external oscillator feeding on the XIN pin of the PMIC, plays a significant role in the longevity of battery life during the suspend/sleep states. The SiT15xx family is a new generation of silicon MEMS 32 kHz oscillators from SiTime that offer a power-saving alternative to traditional on-chip oscillators, external quartz oscillators or quartz crystals (XTALs).

In mobile devices, the 32.768 kHz XTALs can be replaced with SiT15xx oscillators to further lower power consumption. These MEMS oscillators have a low power output with 750nA core supply current (typical). The SiT15xx have additional power savings features such as operation down to 1.2V, programmable frequency down to 1 Hz and programmable output swing.

Programmable Frequency

The SiT15xx oscillators have programmable frequency range between 1 Hz and 32.768 kHz in powers of two. Reducing the frequency significantly reduces the output load current (C*V*F). For example, reducing the frequency from 32.768 kHz to 10 kHz improves load current by 70%. Similarly, reducing the output frequency from 32.768 kHz down to 1Hz reduces the load current by more than 99%. (See examples in the next section.) Quartz XTALs, due to the physical size limitations of the resonator at low frequencies, cannot offer frequencies lower than 32.768 kHz.

Programmable Output

Another power saving feature available with the latest generation of MEMS-based oscillators is NanoDrive™, a programmable output swing. This feature allows the output swing to be programmed to a lower voltage swing and match the PMIC/chipset as shown in **Figure 3**. This programmable output stage minimizes power and maintains compatibility with the downstream oscillator input. The output swing is programmable from full swing down to 200 mV, to consume up to 40% less power than full swing LVCMOS.

No Load Supply Current

When calculating no-load power, the core and output driver components need to be added. Since the output voltage swing can be programmed for reduced swing between 200 mV and 800 mV, the output driver current is variable. Therefore, no-load operating supply current is broken into two sections, core and output driver.

Total Supply Current with Load

The additional load current comes from a combination of the load capacitance, output voltage, and frequency (C*V*F). Since the SiT15xx includes NanoDrive reduced swing output and a selectable output frequency down to 1 Hz, these two variables will significantly improve load current. Power is reduced by greater than 40% with NanoDrive, and reducing the output clock frequency reduces the load current significantly.

The battery in a mobile device looses more capacity during long suspend/sleep states than during its active state. The major contributors to battery drain in low power states are the power and battery management circuits clocked by a 32 kHz time-keeping oscillator. The best solution for conserving battery capacity during suspend/sleep states is to leverage power saving schemes offered by devices such as micro-power consuming programmable silicon MEMS oscillators. By programming the frequency and output voltage of this new class of oscillator, current consumption can be significantly lowered depending on the specific power management implementation in the mobile device.

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The gold in green tech is also measured in jobs

By: Alix Paultre, Editorial Director, PSD

Supporters of "green" technologies, especially in the power space, often stress the financial payback of regenerative-energy systems, more efficient electronics, and intelligent power management. Another very important aspect of green power infrastructures is that they encourage manufacturing and employment.

A system using alternate energy or advanced control methodologies may cost more than legacy solutions, but that expense is mitigated both by performance advantages and cost-of-ownership issues. Add to that the fact that someone must design and manufacture the advanced systems and devices involved in those systems to make them "green", and you have incentives beyond a love of the ecology to support next-generation power systems development.

Those jobs and manufacturing opportunities are ways to recapture sagging middle-class incomes in nations challenged by global trade issues. Precision devices need talented designers and manufacturers with accurate tools and processes to compete at the world-class level. Addressing applications from grid-level infrastructures to personal luxury items, the market for next-generation advanced products powered by green technologies promises to be good for the design engineering community.

According to Roland Berger, the worldwide market for green technology has grown by 11.8% a year on average since 2007, and is now worth over EUR 2 trillion. By 2025, they believe it will more than double to EUR 4.4 trillion. That's a market almost completely open for competition, as the core technologies and infrastructures are only now just being commercialized and the current industry leaders cannot count on their existing market share maintaining in the face of disruptive market developments.

This technology progression has no boundaries in scale or scope. Everything that uses power can use it more efficiently, with cost and effort being the primary obstacles. Using the proper technologies we can generate significant amounts of power from environmental sources such as water, wind, geothermal, and the sun. Even personal devices will eventually be able to power themselves from harvested energy; it is already starting to happen in the area of self-powered sensors in medical monitoring applications.

The key is that there are multiple forces driving our society to a greener and more technically sophisticated one. Advanced power generation, storage, and management technologies are making green tech viable in products and services that provide real cost-effective solutions. Add to that the a future where every major power producing and storage system as well as every power consuming system in developed countries will eventually be linked to one for both power and management efficiency as well, and you have an opportunity for those willing to seize it.

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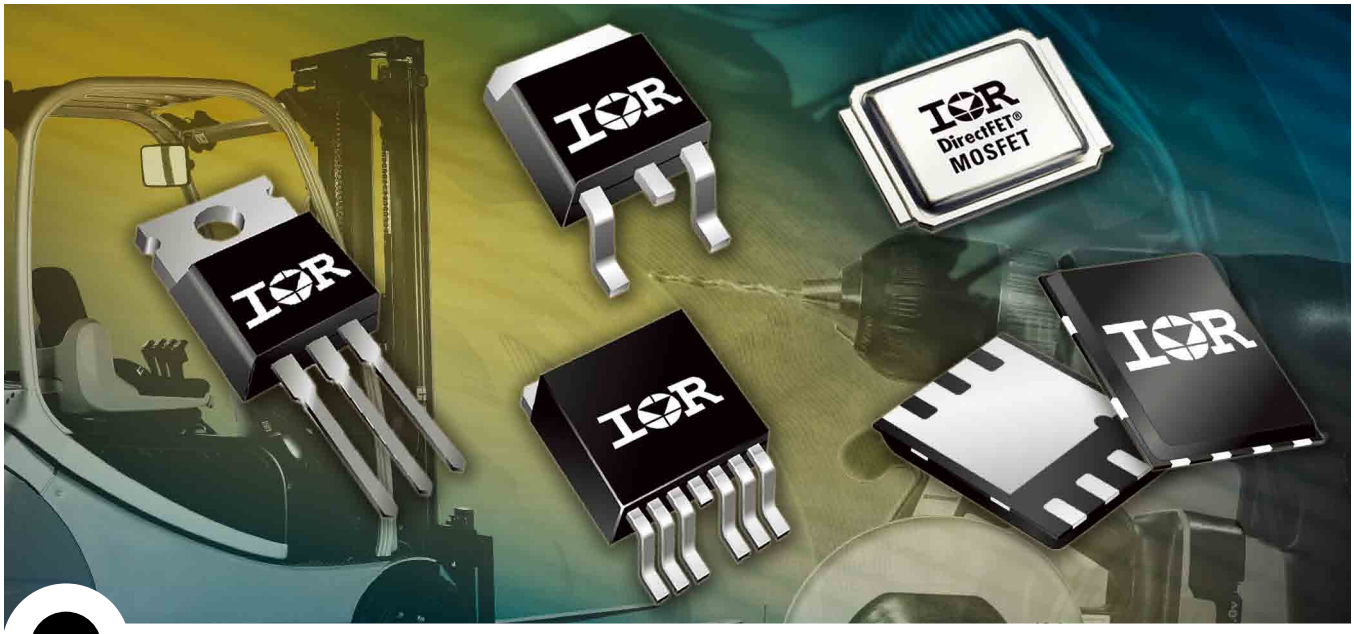

StrongIRFET™ Rugged, Reliable MOSFETs

Specifications

Part Number	B_{VDSS}	ID@ 25°C	$R_{DS(on)}$ max@ Vgs = 10V	Qg@ Vgs = 10V	Package
IRFH7004TRPbF	40 V	100 A	1.4 mΩ	134 nC	PQFN 5x6
IRFH7440TRPbF	40 V	85 A	2.4 mΩ	92 nC	PQFN 5x6
IRFH7446TRPbF	40 V	85 A	3.3 mΩ	65 nC	PQFN 5x6
IRF7946TRPbF	40 V	90 A	1.4 mΩ	141 nC	DirectFET Medium Can
IRFS7437TRLPbF	40 V	195 A	1.8 mΩ	150 nC	D^2-Pak
IRFS7440TRLPbF	40 V	120 A	2.8 mΩ	90 nC	D^2-Pak
IRFS7437TRL7PP	40 V	195 A	1.5 mΩ	150 nC	D^2-Pak 7pin
IRFR7440TRPbF	40 V	90 A	2.5 mΩ	89 nC	D-Pak
IRFB7430PbF	40 V	195 A	1.3 mΩ	300 nC	TO-220AB
IRFB7434PbF	40 V	195 A	1.6 mΩ	216 nC	TO-220AB
IRFB7437PbF	40 V	195 A	2 mΩ	150 nC	TO-220AB
IRFB7440PbF	40 V	120 A	2.5 mΩ	90 nC	TO-220AB
IRFB7446PbF	40 V	118 A	3.3 mΩ	62 nC	TO-220AB
IRFP7430PbF	40 V	195 A	1.3 mΩ	300 nC	TO-247

Features:

- Ultra low $R_{DS(on)}$
- High current capability
- Industrial qualified
- Broad portfolio offering

Applications:

- Battery Packs
- Inverters
- UPS
- Solar Inverter
- DC Motors
- ORing or Hotswap

For more information call +49 (0) 6102 884 311
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