January/February 2011

PSD EUROPE

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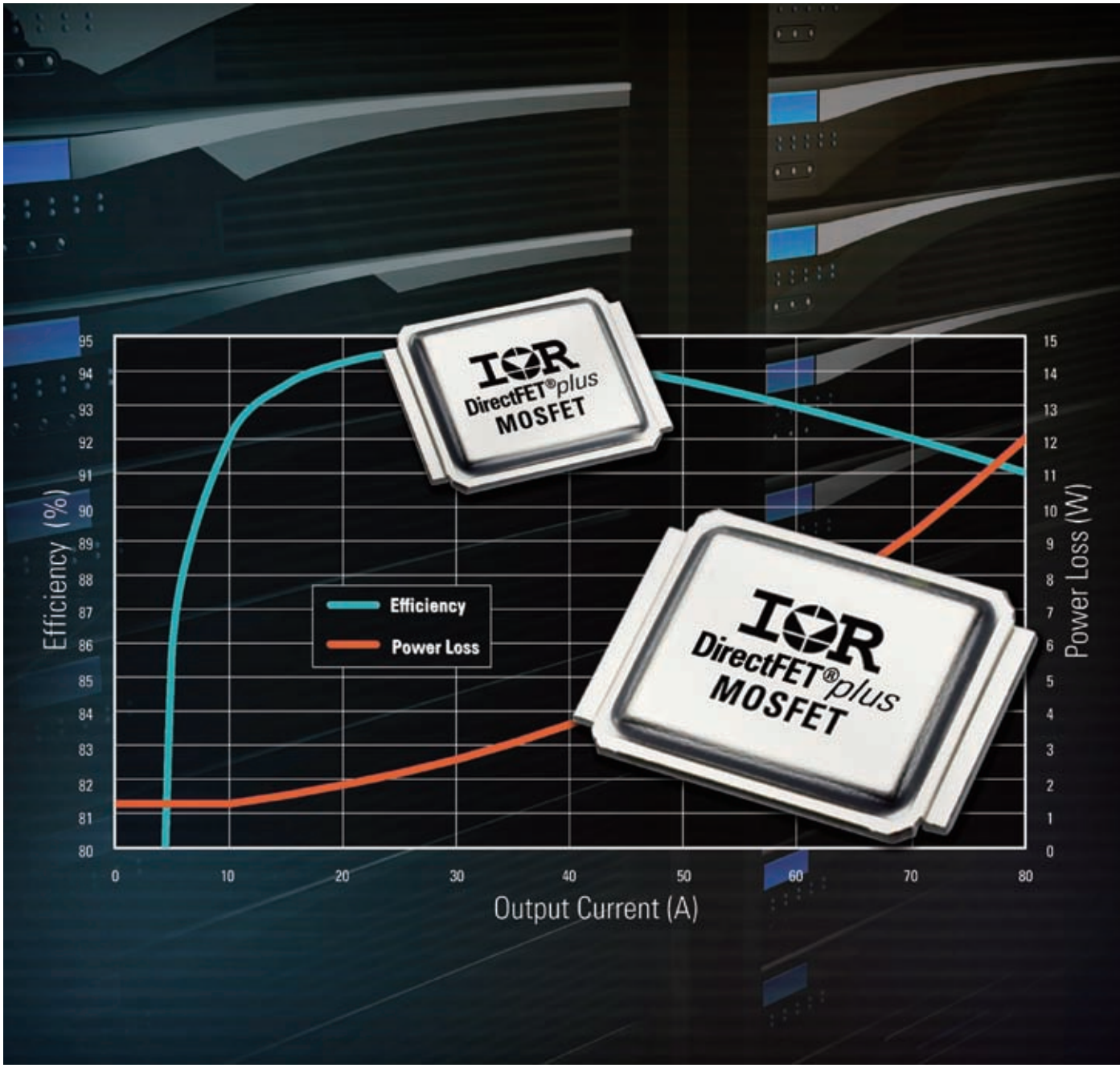

SPECIAL REPORT: ENERGY EFFICIENCY (Pg 29)

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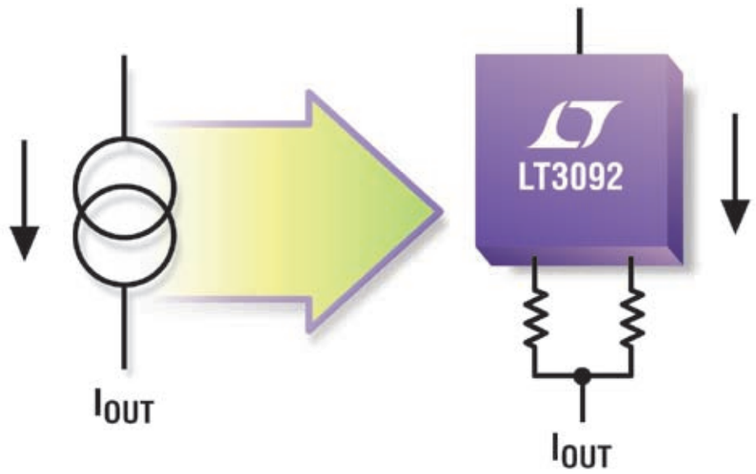

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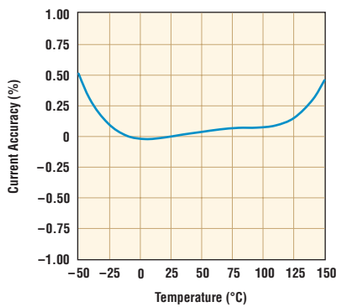

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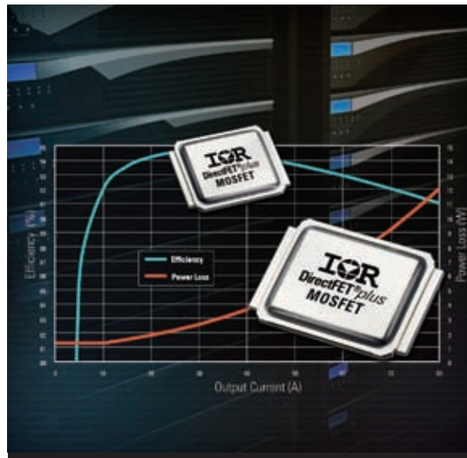
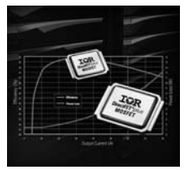


COVER STORY
MOSFET Efficiency (pg 18)



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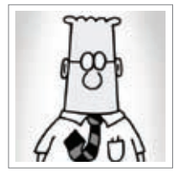

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Volume 8, Issue 1

LOOKING FORWARD... LOOKING BACK

Welcome to this issue of PSD where we carry a feature on energy efficiency. With the uncertain and sometimes unstable future of our traditional energy sources, plus the concern over the pollution of our environment, energy efficiency has never been so important. All designs for electronic equipment now have this as a major consideration and power has never been such a vital part of the overall design process.

The outlook is optimistic for Europe's power sector in 2011, but opinion is still divided on the business benefits of single European electricity market. Energy and utilities firms have expressed optimism concerning the growth prospects for Europe's electricity market in 2011. A poll of 60 power equipment and service providers and their customers undertaken at POWER-GEN Europe 2010 found that the majority of respondents (75%) see a strengthening in market demand next year, despite the uncertainty surrounding international climate change regulation. Indeed, only 1.5% thought the market would weaken.

Industry opinion remains divided regarding the impact of climate change regulation, and that of the EC's common European electricity market proposal, with a third of respondents believing the uncertainty surrounding international climate change regulation was having a negative impact on the European power industry and just under a third believing that it would benefit their business.

A proposed mandate from the U.S. Department of Transportation will cause sales of new cars with rear-view park assist cameras in the country to quadruple compared to previous expectations during the next seven years, according to the market research firm iSuppli, now part of IHS Inc. The mandate calls for all new motor vehicles weighing less than 10,000 pounds (4,545kg) sold in the United States to incorporate backup cameras by Sept. 1, 2014. The cameras are designed to eliminate blind spots behind cars that contribute to back-over collisions.

Because of this, all new cars sold in model year 2015 are expected to include rear-view park assist cameras, up from iSuppli's previous forecast of only 20%.
The projection from iSuppli predicts that from 2011 through 2017, 71.2 million new cars in the United States will be sold with rear-view cameras for park assistance. The pre-mandate forecast predicted only 19.1 million for the same period.

With the U.S. market beginning to accelerate dramatically in 2012, sales will rise 119.9% to 2.8 million units, up from 1.3 million units in 2011. Sales then will increase by 117.4% in 2013 to reach 5.98 million, and will climb another 91.1% in 2014 to hit 11.4 million. By 2017, a total of 17.1 million cars, representing the entire estimated new-vehicle fleet, will be sold with rear-view cameras in the United States.

I hope you enjoy this issue, and I look forward to seeing many of you at APEC in Dallas. Please keep your valuable feedback coming in. We have redesigned the magazine and website to make PSD what you want it to be. It's your magazine.

All the best!

Cliff
Editorial Director & Editor-in-Chief, Power Systems Design
Cliff. Keys@powersystemsdesign.com

MACHXO2 LOW COST, LOW POWER PLD

Lattice Semiconductor Corporation's new MachXO2™ PLD family, offers designers of low-density PLDs an unprecedented mix of low cost, low power and high system integration in a single device.

Built on a low power 65-nm process featuring embedded Flash technology, the MachXO2 family delivers a 3X increase in logic density, a 10X increase in embedded memory, more than a 100X reduction in static power and up to 30% lower cost compared to the MachXO™ PLD family. In addition, several popular functions used in low-density PLD applications, such as User Flash Memory (UFM), I2C, SPI and timer/counter, have been hardened into the MachXO2 devices, providing designers a "Do-it-All-PLD" for high volume, cost sensitive designs.

The MachXO2 family offers three options for maximum flexibility. MachXO2 ZE devices range from 256 to 7K look-up tables (LUTs), operate off a nominal 1.2V power supply, and support system performance up to 60MHz. With power specified as low as 19uW and packages as small as 2.5mmx2.5mm, the MachXO2 ZE devices are optimized for cost-sensitive, low power consumer design applications such as smart phones, GPS devices and PDAs.

MachXO2 HC devices range from 256 to 7K LUTs, operate off a nominal 3.3V or 2.5V power supply, and support system performance up to 150MHz. Offering up to 335 user I/O and a robust design solution (instant-on, non-volatile, input hysteresis and single-chip), these devices are ideal for control applications in end markets such as telecommunications infrastructure, computing, industrial and medical equipment.

MachXO2 HE devices range from 2K to 7K LUTs, operate off a nominal 1.2V power supply and support system performance up to 150MHz. These devices are optimized for power sensitive system applications.

Customers can start designing with MachXO2 devices today using Lattice Diamond™ v1.1 software, which can be downloaded for free from the Lattice website at www.latticesemi.com/latticediamond/downloads/

Existing ispLEVER® software users have the option to use the free ispLEVER v8.1 SP1 Starter software, downloadable from the Lattice web site, with an installed control pack. Visit www.latticesemi.com/starter.

In order to enable quick and efficient design and deployment of commonly used functions in system and consumer applications, more than 20 reference designs using MachXO2 devices can be downloaded for free from the Lattice website.

In addition, Lattice plans to make available two development kits that accelerate the evaluation of MachXO2 devices.

Pricing for the LCMXO2-256ZE/HC TQFP100 is $0.75 and the LCMXO2-1200ZE/HC TQFP100 is $2.00, both in 500KU volume. All members of the MachXO2 family are expected to be shipping in production by the end of Q3 2011.

For more information, visit www.latticesemi.com/machxo2devkits.

www.latticesemi.com

EFFICIENCY TRENDS IN POWER SUPPLY DESIGN

By Ralf Regenhold

Much has changed in 30 years of power supply design. Take for example a seemingly very simple design task: Generate a 5V/1A regulated output from a typical industrial bus voltage of 24V. 30 years ago when linear regulators became popular, the approach would not have even been possible due to high power dissipation.

Transformers would be used for generating an output voltage as close as possible to the desired load voltage in order to minimize the voltage drop and power dissipation across the LDO. Overall efficiencies were in the range of only 40%. The need for higher load currents forced engineers to increase efficiency and improve thermal management. They started to use switch mode power supplies.

Then, about 20 years ago, the concept of "Ease of Use" in buck regulator design was introduced and branded "SIMPLE SWITCHER®" integrating the switch and featuring a simple design methodology. This allowed a drastic total solution size reduction by removing the transformer and large heat sinks. Using the above-mentioned design example, the first family LM257x was already achieving on an efficiency of 82% at a solution size of 800mm².

The second generation SIMPLE SWITCHER set the next trend in power supply design by the customer's demand of cost reduction while further increasing the efficiency to 84% in our example and a reduction of the solution size. Shorter design cycles were possible by using a design software which replaced the manual calculation.

During the following years, advanced silicon technologies allowed a further increase in switching frequencies which lead to reduced sizes of the inductor and capacitors. Smaller overall size factors have been achieved, but this has introduced a further problem; insufficient air-flow, leading to higher operating temperatures thus reducing the lifetime of the system. To avoid this problem, further improvements of efficiency were required.

The latest trend today is towards minimum solution size at very high ambient temperatures. In addition, load current requirements are constantly increasing. Actual regulators are therefore designed for maximum efficiency and maximum integration. Ease of manufacturing and layout is required to address the requests for testability, mechanical robustness and avoiding any problems in electromagnetic emissions. All these requirements are met by the today's approach of SIMPLE SWITCHER Power Modules (LMZ series) which can achieve an efficiency of 90% at a solution size of 370mm² with an ambient temperature of up to 110°C.

Another aspect of efficiency in a power management project is time-to-market. Short design times lead to lower development costs, higher flexibility on high value custom solutions and faster revenue generation on new product releases. To address this need, National Semiconductor introduced a web-based design tool, WEBENCH®, which generates reliable power supply designs in seconds and allows analysis and optimization according to design requirements.

In addition to a constant increase of efficiency at the point of load regulator, the total system energy management is becoming the next focus. Systems which are based on modular concepts like blade servers, storage networking systems, routers & switches, in telecom or factory automation, benefit from a dynamic and intelligent energy management system. Individual subsystems which are not loaded can be turned off. Others, which are overloaded and therefore not operating at the highest power efficiency need load sharing support from a subsystem running at low load. Here, devices like the LM25066 are capable of hot swap control with power limiting, simultaneous measurement of subsystem input voltage and current and the delivery of a true power measurement and temperature measurement. A digital interface monitors and controls those parameters in real-time.

After looking at over 30 years of efficiency improvement, we need to move forward from single chip optimization towards system optimization by using high efficiency devices supported by sophisticated algorithms in the very latest, high-performance design tools.

Author: By Ralf Regenhold
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DRIVE TO ENERGY EFFICIENCY CREATES NEW OPPORTUNITIES

By Ash Sharma

Some may view the power electronics industry as notoriously slow to change. Perhaps in the past this has been true, but certainly not any longer when you consider the rapid advances being made towards better energy efficiency and energy savings in industry, the workplace and the home.

I wrote on the topic of energy efficiency a year ago, highlighting the achievements of the industry over the past decade regarding energy savings, and looking back over the past 12 months, I can see that further small, but important steps have been made towards the goal of a low-carbon environment.

In the last 2-3 years, suppliers in the power electronics industry have had to grapple with the effects of the global downturn and the subsequent rapid recovery and allocation situations in 2010. However, this period of instability did give suppliers a chance to reflect, reorganize and re-strategize with an increasing focus for many suppliers on "new" markets, almost all of which are linked to energy savings and efficiency.

Some of the more significant changes in the industry last year included the rise of the full electric vehicle, the advancement of "smart" appliances for the home, the massive surge in new solar installations, the on-going shift to more efficient lighting, and the introduction of a universal charging standard for mobile phones.

Almost all major vehicle manufacturers have announced plans to release an electric vehicle. Two suppliers, Nissan and GM went even further, releasing their Leaf and Chevrolet Volt models respectively in 2010, and selling not insignificant volumes last year. If volumes of such vehicles rise into the millions per year as expected, this will create huge growth opportunities, both within the drivetrain and associated battery technology, and also in the charging infrastructure required to support these vehicles.

During January's Consumer Electronics Show in Las Vegas, we witnessed several major companies, including the likes of LG and Samsung, announce plans to release "smart" appliances. These products not only offer the consumer greater functionality, such as remote control via a smartphone, but also aim to reduce energy consumption costs, by using smart meters and a Wi-Fi connection to take advantage of off-peak electricity rates. These announcements reflect a broader trend towards a "connected home" which will allow consumers to take a more active role in reducing their energy usage.

Fossil fuels and nuclear technologies continues to rule the energy generation world, but further steps were made in 2010 to increase the proportion that came from renewable energy sources. Wind power capacity continued to expand, and for the first time, China actually overtook the US, in terms of newly installed capacity, indicating China's important future role in the market's development. Solar power, which has always been wind power's smaller brother, also enjoyed a major growth spurt in 2010. Newly installed capacity of around 17GW in the year, helped to nearly double total capacity to some 35GW. Utilities in Germany, the major driver of new installations last year, claimed that solar power now handles 20% of the country's peak power requirements. As the capacity of both wind and solar increases, so does the opportunity for power component vendors. The push towards energy storage in the grid, accelerated by vast numbers of renewable energy generators presents further major opportunities.

Another major change in 2010, which will affect the consumer, is the European Commission's recently introduced "Universal Charging Standard". The standard which was backed by 14 of the top handset suppliers intends to reduce wastage of mobile phone chargers by having a single micro-USB protocol for all new handsets. This presents one of the few developments in the industry that may in fact reduce power electronics opportunities due to restricting charging volumes and associated power component content.

These few examples demonstrate just some of the recent developments in the power industry relating to energy usage. The full list is much larger and should provide massive new opportunities for many companies in 2011 and beyond.

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POWER SUPPLY DEVELOPMENT DIARY

Part X

By Dr. Ray Ridley

This article continues the series in which Dr. Ridley documents the processes involved in taking a power supply from the initial design to the full-power prototype. In Part X, Dr. Ridley presents the rules for good PCB layout.

PCB Layout

In part IX of this series, an example was given of a crucial area of PCB layout around the control chip. This illustrated the details that need to be taken care of when laying out a switching power supply and its control circuit. Further examples of how to take care of specific issues on individual power supplies could take an entire book, something that is well beyond the scope of this design series. However, it is worth taking some time to highlight the important issues to be concerned with when laying out a switching power supply.

There are nine fundamental rules that should be followed for a switching power supply board:

Rule Number 1: Use at Least a 2-Layer Board

The cheapest possible power supplies use single-sided boards and jumpers where necessary. While this can be done, it makes a designer's life extremely difficult. The preference is to use at least two layers. This provides much more design flexibility and a tighter, better performance and more rugged layout.

If working with more than two layers, it is advisable to keep critical power paths on the top and bottom layers where they can be clearly seen, and sometimes repaired in the event of failures during the development program. If inner layers are used, they should be properly spaced from each other, as discussed in Rule number 5 below.

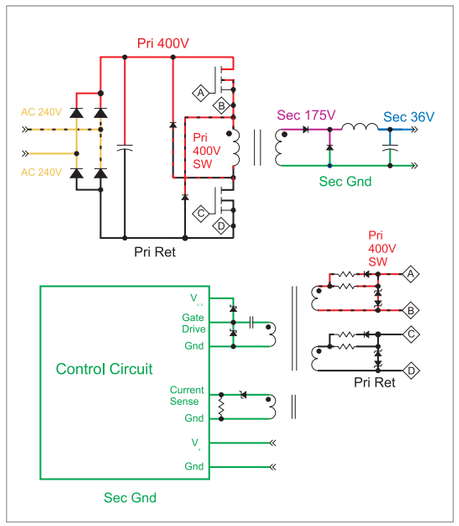

Figure 1: Simplified Forward Converter Schematic with Trace Voltages .

Rule Number 2: Draw the Schematic Properly

There are several functions of a schematic: the first is to establish all connections properly for the CAD system, ready for the layout program. If schematic drawing is left in the hands of CAD designers with no power supply knowledge, this is the only thing that really matters to them. However, this ignores the other functions of the schematic.

A clear schematic of a power supply should clearly delineate the power stage topology, control circuits, and isolation areas. A the type of technology being used for the power stage and control circuit. Many times, schematics are drawn in such a way that it is difficult to even identify which power topology is being used.

The schematic is also used to troubleshoot problems. Proper placement of components on the schematic should be logical relative to where they are placed on the board, and this speeds up the troubleshooting process.

Finally, the schematic should be used as a guide for showing the critical paths in the circuit, and should help you identify the crucial regions discussed in the layout considerations listed below. The schematic is the document on which you can sketch out the voltages, currents, and crucial paths, allowing you to think ahead about how the layout will be done.

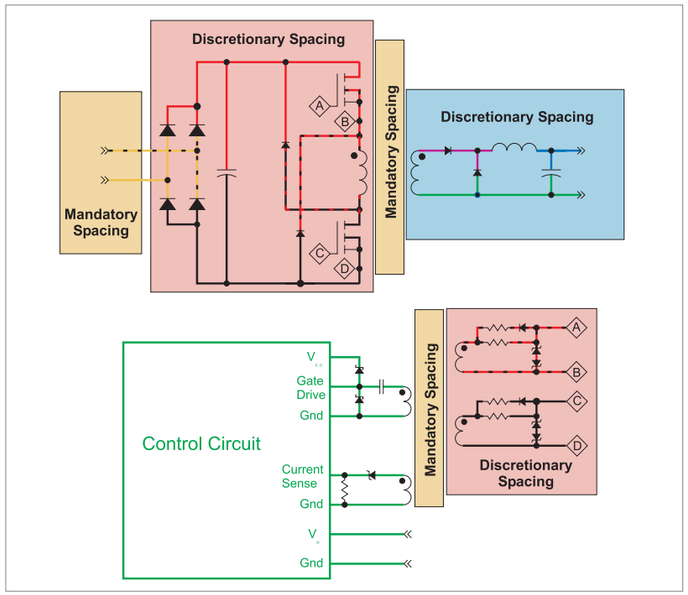

Figure 2: Simplified Forward Converter Schematic with Spacing Guidance.

Rule Number 3: Place All Power and Control Components Manually

Power and control components should be manually placed and oriented to facilitate the subsequent placement of traces. A proper schematic will show the appropriate components next to each other, and aid in the initial placement of the components. This work should always be done by someone with power supply design experience, and preferably by the engineer who is most familiar with the specific power supply being laid out. As the routing is done, it is not uncommon to change a component placement in order to optimize the layout.

Rule Number 4: Place Traces Manually

Experienced designers do not attempt to use autorouting for their power supply components. All critical power traces are placed by hand, allowing the designer to think about the optimal placement for minimizing EMI. Even the best modern CAD systems are inadequate for laying out switching power supplies automatically.

Rule Number 5: Use Proper Spacing for High Voltages.

A common mistake in the PCB design of many power supplies is inadequate spacing between traces, especially in the areas of the circuit where there are no specific agency rules that must be followed.

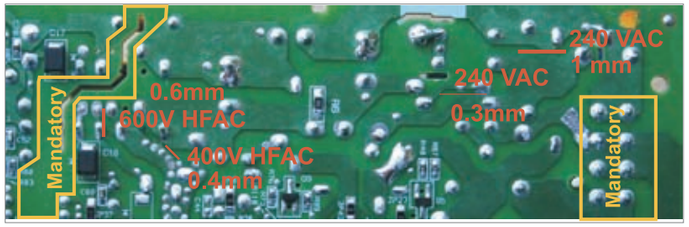

Figure 3: Example Preproduction Power Supply Board with Inadequate Spacing.

Figure 1 shows the forward converter schematic, simplified to a single output stage to illustrate the issues that arise with voltage spacing. The voltages that can exist on each trace are marked in different colors on this schematic.

Notice that there are multiple areas on the primary part of the schematic that can see up to 400 V, either DC, or with high-frequency switching. Careful attention must be paid to each of these areas in layout to prevent the possibility of voltage breakdown and failure in the power supply.

The secondary side of the circuit can also have high voltage potentials, especially at the output of the transformer. When assessing these voltage levels on your schematic, remember that you must include the high-frequency switching spikes that can occur, not just the anticipated square-wave voltages. Hence the voltage noted on the secondary of this converter is as high as 175 V.

Despite the fact that high voltages exist at many points in a typical power supply design, there are surprisingly few hard rules for laying out a PC board. As shown in Figure 2, the safety agencies are only concerned with two areas on the board – the raw incoming AC power traces, and the separation of traces between the primary and safety-voltage secondary of the converter.

In these two areas of the converter design, there are very specific requirements for the distances between traces and component pads. On the primary side, with 240 VAC applied, the rules typically call out 2-3 mm of spacing, the actual number depending on the industry you are designing for. Free air has a typical breakdown rating of 1000V/mm, so this requirement provides plenty of margin.

Between primary and secondary circuits, the required spacing is even larger – typically 6 mm or more depending upon the particular application you are working on. It is very important that you clearly show this safety boundary area on your PC board, providing a clear path through all layers of the PCB. When held up to the light, the safety spacing should be apparent.

Once the input traces are separated from the AC input line by a component (which presumably can fuse for protection) there are no longer any safety requirements, and board spacing is strictly at the discretion of the layout designer. Also, on the secondary side of the converter, there are not any specific specifications for layout spacing.

Despite the lack of direct safety agency guidance, common sense should be applied to the parts of the circuit with high voltages between them. The 2-3 mm rule that is applied to the AC line exists for a reason – this extra spacing allows for nonideal situations such as condensation and contamination on the board. On the primary side, it is always a good idea to keep as much spacing as is reasonable, preserving the 2-3 mm if possible. For some power components, this is not always possible or practical, and the spacing must be compromised.

On the secondary side, also, do not immediately revert to CAD system minimum trace separations. You should always look at the actual voltages seen in the circuit, and space the traces and components accordingly.

Many companies have their own internal guidelines, and these should be followed carefully wherever possible. If your company does not have these, then common sense should prevail. If you have 1000 V between two traces, don't put them just 1 mm away from each other. Even with conformal coating on a board, there is usually no reason to make the spacing so small.

Figure 3 shows an example of a pre-production power supply where discretionary spacing issues were ignored on the PCB layout. The mandatory rules were adhered to in the primary spacing, and the safety spacing areas, so the board would pass agency inspection. However, in this example, some of the discretionary spacings are so small that breakdown of air is possible even though the initial prototypes worked fine. This particular board was modified before production to increase the crucial spacing areas.

In reviewing power supply designs over the last couple of decades, I have seen this to be a very common error. Modern tiny packages have exacerbated the issue. Another insidious problem that can exist is when inadequate spacing is provided between high-voltage traces on inner layers of a PCB. Inexperienced designers may be counting on the insulation of layers for protection, but lateral failures can occur on inner layers if insufficient spacing is used.

Summary

There are nine basic rules for laying out a PCB for switching power supplies. Five of them have been covered in this article, with special attention applied to the proper voltage spacing between PCB traces. The remaining four rules, involving the routing of traces, and placement of planes, will be covered in the next article of this series.

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Author: Dr. Ray Ridley
President
Ridley Engineering

www.ridleyengineering.com

DELIVERING 'WHAT'S NEXT'

Mouser beams in on energy-efficient technologies

Reported by Cliff Keys

In keeping with its philosophy of bringing "What's Next" to the engineering marketplace Mouser Electronics, Inc. is taking the lead in providing new energy-friendly technologies to meet growing demand for high-performance components with lower energy consumption. Russell Rasor, Vice President of Advanced Technology at Mouser Electronics, Inc. explained the detail.

The company's Advanced Technology Group is concentrating on energy-harvesting components and solid-state lighting, as well as leading-edge advancements in ultra-efficient MCUs to stay at the forefront for design engineers.

In the area of energy management, the industry has seen a huge movement towards components with lower-power consumption, where the newest 32-bit microcontrollers can consume one quarter of the energy of other 8-, 16- and 32-bit MCUs. Mouser stocks low-power MCUs from such top manufacturers as Texas Instruments, ST Microelectronics and Microchip, to name a few. The trend to reduce power consumption and extend battery life continues to escalate, and Mouser is keenly focused on being able to deliver those cutting-edge technologies to design engineers. In addition, with 14 global customer support locations, the company is providing important product data assistance to help engineers across the world bring their ideas to market faster.

In the quest to find alternative energy sources, the buzz centers around micro energy harvesting, which captures tiny amounts of energy from the environment through vibration (piezoelectric and oscillating mass), temperature (TEGs or thermoelectric generators), light (solar panels) and RF (induction through ambient electro-mechanical waves), among other sources. For example, such harvesting can make the operation of wireless sensors virtually maintenance-free over the long term. In fact,

Mouser Headquarters, Mansfield, Texas, USA

this trend is projected to become a leading power source for many of tomorrow's wireless devices. An estimated 200 million energy harvesters and thin-film batteries will be in use by 2012, according to The Darnell Group, a market research firm. The market for automotive, home, industrial, medical, military and aerospace energy harvesting applications is expected to grow from 13.5 million units in 2008 to 164.1 million units by 2013. For information on the latest alternative energy products, visit www.mouser.com/knowledge/alternate_energy/.

Energy harvesting from a natural source, where a remote device is deployed and its natural energy source is essentially limitless, has become an increasingly attractive alternative to inconvenient wall plugs, costly batteries and the like, explained Russell Rasor, Mouser Vice President of Advanced Technology. "Since this energy source is basically free, it is sparking the attention of the design engineers. Plus, the cost of harvesting has now decreased to the point where it is a practical alternative to traditional power sources," Rasor added.

A harvesting system can be composed of multiple components that efficiently and effectively capture, accumulate, store, condition and manage this energy, and supply it in a form that can be used in various applications. Some examples of this can be found in thermal meter reading for HVAC systems or humidity sensors in agriculture. Viable low-leakage storage options include conventional rechargeable batteries, as well as newer thin-film batteries, ultra capacitors and EDLCs (electrochemical double-layer capacitors). When designed and installed properly, this energy source is available throughout the lifetime of the application, hence the advantages, Rasor continued.

Mouser's Advanced Technology Group is also offering support to key applications in energy-efficient lighting. At the forefront is SSL (solid-state lighting), including LEDs (light emitting diodes), OLEDs (organic light emitting diodes) and PLEDs (polymer light emitting diodes). The LED market is predicted to account for 16% of the worldwide lighting market by 2013 and will generate over $20 billion in revenue in the United States alone. The upcoming sales ban on incandescent light in a number of countries, including the US and Canada, is fueling the LED movement, too, Rasor explained.

SSL will continue to take the place of existing lighting solutions in industrial, commercial and residential applications because they offer more brightness per watt while producing less heat eliminating the need for heat management solutions. The lifespan, flexibility and variety of these new SSL options provide value-added benefits for design engineers as they seek improved technologies, which in the end, will offer tremendous benefits to the consumers of tomorrow.

"Along with providing these emerging technologies, Mouser is committed to producing solution-based content on its website as a resource to the design community," Rasor stated. "These are all technologies that require much more than a list of part numbers. We provide downloadable data sheets, supplier-specific reference designs, application notes, technical design information and engineering tools."

Mouser has created a Light

Russell Rasor, Vice President of Advanced Technology at Mouser Electronics, Inc.

Application Center section of the Knowledge Center on its website, www.mouser.com/Application_lighting to help the design community further aid new development. "We want to provide more guidance to help customers select the correct components to fit their design requirements. Our goal is to help our customers be at the forefront of 'What's Next'," Rasor added.

Mouser Electronics, Inc., part of Berkshire Hathaway, Inc. is known as a leading global design engineering resource for emerging technologies and products. The company's extensive website, www.mouser.com features more than 1.8 million products online from more than 400 manufacturers. Mouser currently has 14 global customer support centers and the company offers fast global shipping to over 300,000 customers in 170 countries from its 492,000 sq. ft. state-of-the-art facility in Texas, USA.

Author: Reported by Cliff Keys
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MOSFET EFFICIENCY

Silicon improvements drive performance with DirectFET plus

By Omar Hassen and Vijay Viswanathan

Improvements in silicon performance - including process structures that improve on-resistance and lower gate resistance (Rg) - are being combined with optimal package technology to improve the efficiency, reliability and thermal performance of next-generation power MOSFETs.

High energy prices and the increasing profile of "green" initiatives such as Energy labeling for appliances and the Energy Star 80 Plus scheme for electronic products are creating a strong pull for improvements in power MOSFETs that increase DC-DC conversion efficiency in servers, notebooks, high-end desktops and other computing, datacenter and networking applications. At the same time, end-user demands for extra functions, richer experiences and smaller dimensions require devices supporting greater power density and increased reliability.

So far, great strides have been achieved, in terms of MOSFET packaging and device design, to meet these wide-ranging demands. Coming generations of power MOSFETs will combine high performing package technology with the latest advances in silicon to take power conversion efficiency to the next level, particularly for applications that demand higher frequency operation. As well as making further improvements in areas such as On-resistance $R_{DS(on)}$ and gate charge Q_g, new MOSFET process structures that lower MOSFET gate resistance (Rg) and improve resistance/active area (R^*AA) figures of merit play an increasingly important role in delivering additional improvements to synchronous converter efficiency.

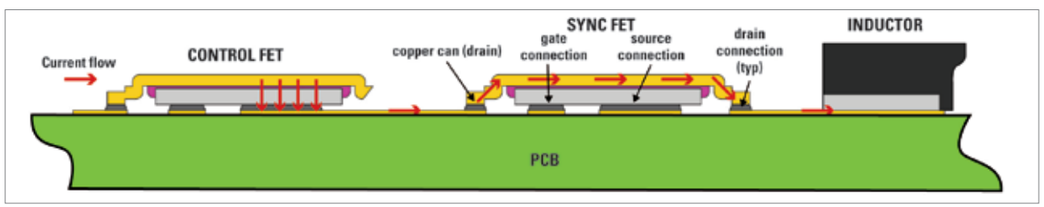

Figure 1: DirectFET package construction and implementation

Optimizing Package Performance

Surface-mount power packages have evolved through several generations since the arrival of the first SO-8 Power MOSFETs in the early 1990s. Techniques such as double-sided cooling, large metal leadframes and clip bonding to die-level ohmic contacts have all been developed to minimize the effects of thermal resistance from junction to case (RTHj-c) and to combat electrical loss mechanisms such as Die-Free Package Resistance (DFPR) and parasitic inductances. Successful power packages include IR's leadless Power QFN (PQFN) for small-footprint applications.

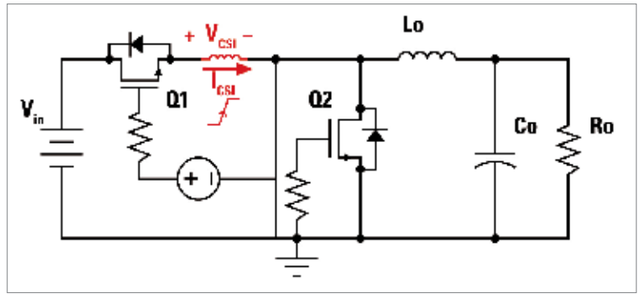

Figure 2a: Effect of source inductance at turn on.

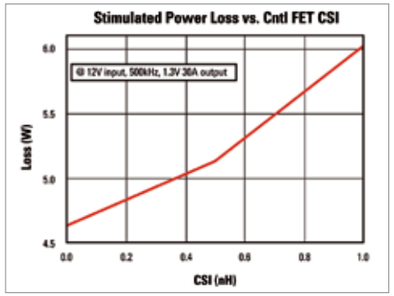

Figure 2b: Effect of Ls on power loss

Among the most effective packages for power MOSFET design has been International Rectifier's DirectFET®. In particular, the simplicity of the package construction, with fewer interfaces when compared, for example, with PQFN alternatives, makes DirectFET an attractive solution for applications where reliability is a primary design requirement. The latest generation of IR's DirectFET package technology delivers close to ideal performance by combining techniques to minimize RTHj-c and reduce DFPR to a level insignificant relative to the $R_{DS(on)}$ of the MOSFET die. The DFPR, as well as parasitic inductances, have been successfully reduced through simplified construction, which minimizes the number of materials through which the current must pass. The cross-sectional diagram of figure 1 illustrates the features of DirectFET packaging technology, which combine effectively to minimize the key electrical and thermal parasitic effects.

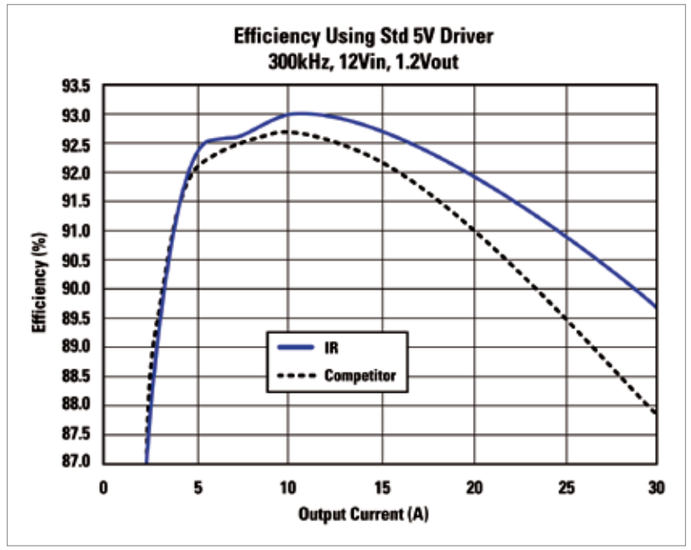

Figure 3: Efficiency improvement by reducing MOSFET Rg.

As the diagram shows, the MOSFET die is fabricated with top-layer metal in conjunction with a proprietary passivation system. This creates large gate and source contacts on the surface of the die. The die is then flipped, bringing the terminals into direct contact with the PCB. A top-side copper can provides the connection from the drain on the back of the silicon die to the PCB. This construction eliminates not only the conventional lead frame and wirebonds that lead to high package resistance but also eliminates plastic packaging materials, which have relatively high thermal resistivity compared to the metals used in the DirectFET package.

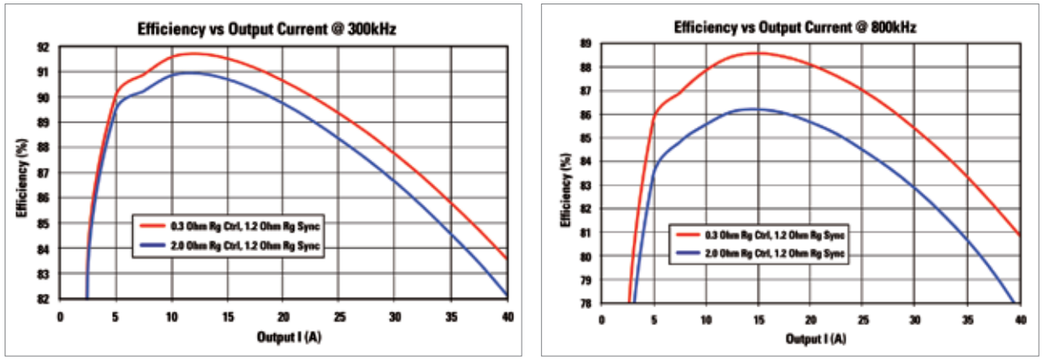

Figure 4: Efficiency measurements at 300kHz and 800kHz.

Using DirectFET packaging helps to both reduce losses and heat generation in the PCB itself. The design maximizes contact area between the source and gate pads and the PCB for best electrical and thermal efficiency, while conduction of drain (load) current through the can rather than through the PCB eliminates effects of I2R losses in PCB traces. This greatly enhances overall efficiency. At the same time, the large copper drain connection provides an alternate path for heat dissipation and provides a very efficient thermal interface to an external heatsink.

In addition, the DirectFET package has extremely low source inductance (Ls), and the large gate and source terminals also allow driver circuitry to be connected without including any PCB stray inductance in the high current path. This results in exceptionally good high frequency switching performance, with improved turn-on and turn-off characteristics and low switching losses in circuits such as synchronous buck converters.

Source Inductance and Switching Loss

Low source inductance helps to reduce switching losses associated with the turn on and turn off of the ControlFET by minimizing the de-biasing effect of the common source impedance in a sync buck circuit. To highlight the benefit of the low source inductance achieved using DirectFET technology, figure 2 shows the effects of Ls when switching the control FET of a synchronous buck converter. At turn on, a voltage drop is induced across Ls as the gate drive voltage increases and the FET turns on. This voltage drop reduces Vgs, thereby impeding the turn on of the MOSFET. This increases the turn-on time of the device and hence increases switching losses.

At turn off an opposite effect is induced that causes the Vgs to increase. This extends the turn-off time and adds further to switching losses. Figure 2b shows the effect of Ls on power loss.

The DirectFET package, combined with effective optimization of the PCB layout, minimizes this effect resulting in improved efficiency and lower heat dissipation. Other parasitic inductances are also significantly lower compared to other packages, contributing to faster transitions and hence lower switching losses. These include the drain-to-source inductance (Lds) and the gate inductance (Lg). Lg is extremely low as the gate is soldered directly onto the PCB.

Next-Generation Silicon Supports Industry-Leading Performance

Clearly, DirectFET technology has enabled a number of significant performance improvements at both package and PCB levels. Improvements at the MOSFET silicon level are more difficult to achieve; processes, architectures and material technologies are already highly evolved, and it is well known that the established techniques for reducing $R_{DS(on)}$ to enhance conduction performance tend to increase the gate charge (Q_g) resulting in higher switching losses.

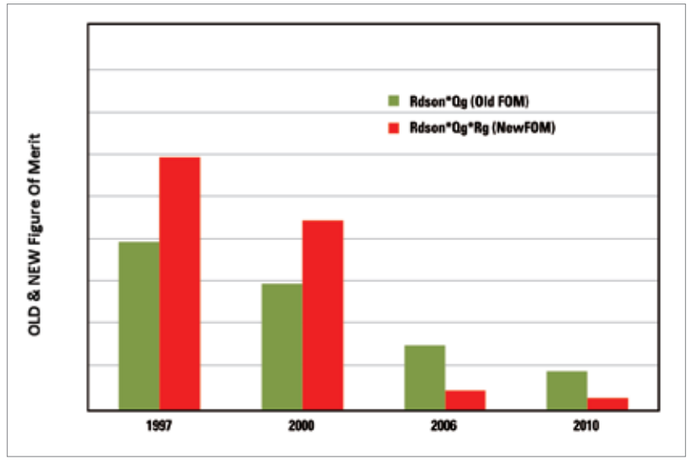

Figure 5: Evolution of MOSFET performance in relation to RDS(on) x Qg and new FOM.

With the emergence of synchronous topologies, which have improved typical buck converter efficiency, MOSFET vendors have been able to maximize these improvements by offering devices as a chipset combining MOSFETs that are individually optimized for control FET and sync FET duties. In these chipsets the control FET is optimized for minimum switching losses, while the sync FET characteristics prioritize low conduction losses.

The trade-off between $R_{DS(on)}$ and Qg has presented a barrier to further improvement of MOSFET performance. Development has focused on optimizing device characteristics based on $[R_{DS(on)} \times Qg]$ as the dominant FOM for power MOSFETs. The latest DirectFET plus family of devices, however, uses new silicon structures that not only further reduce $R_{DS(on)}$ and Qg but also offer industry-leading $R_{DS(on)}$*AA figures of merit while reducing an additional parameter that contributes to power loss, namely gate resistance (Rg).

Effect of Gate Resistance (Rg)

When researching the performance of MOSFETs in synchronous rectifiers operating above 300kHz, IR's engineers found that devices having low Rg would deliver appreciably greater efficiency than competing devices featuring apparently better FOM. Figure 3 illustrates the efficiency measurements taken from two synchronous buck regulators operating with 12V input and 1.2V output, at 300kHz switching frequency and using a standard 5V gate driver. The standard FOM and [Rg x Qg] product for the control FET and sync FET in each design are also shown. Despite having a 35% lower conventional FOM ($R_{DS(on)}$ x Qg), the devices with higher Rg x Qg achieve lower operating efficiency;

The contradiction is due to the fact that the traditional FOM does not take into account the impact of Rg on a number of loss mechanisms, including Cdv/dt on the sync FET, gate driver and dead time.

As a practical illustration, Figure 4 shows how reducing Rg of the control FET has a dramatic effect on efficiency as operating frequency is increased from 300kHz to 600kHz.

Lowering Rg is also effective in preventing Cdv/dt induced turn-on of the sync FET. This spurious turn-on can occur due to the rapid increase in sync FET drain voltage caused by turn on of the control FET. The rapidly increasing voltage induces a voltage spike on the sync FET gate through the device's Cgd capacitance, which can be large enough to turn the sync FET on. Although not catastrophic to the device, Cdv/dt induced turn-on incurs significant losses that are largely independent of load current and therefore impair efficiency throughout the load range. The effects also

compromise the reliability of the converter.

Cdv/dt induced turn-on is typically avoided by ensuring the sync FET has a low gate-to-drain charge, Qgd and a low charge ratio (Qgd/Qgs1). Qgs1 determines the amount of charge required for the gate to move from ground to its turn-on threshold. Qgd is defined as the Cgd charge when the drain voltage rises to 15V. As a rule of thumb, a charge ratio close to 1.0 has been considered sufficiently low to eliminate Cdv/dt turn-on. However, typically a reduction in charge ratio can impact $R_{DS(on)}$. A lower Rg can help to compensate for a higher charge ratio, allowing low $R_{DS(on)}$ to be maintained without increasing the risk of Cdv/dt turn-on.

A further benefit of lowering Rg is to ensure more even turn-on of the MOSFET cells across the die, bearing in mind that power MOSFETs comprise large numbers of cells connected in parallel. Ensuring more uniform turn-on characteristics for the individual cells avoids temporarily exposing a reduced number of cells to the full load current.

Rg and Driver Selection

When the converter designer comes to select suitable gate drivers for the sync FET and control FET, a low Rg increases design freedom and allows a lower cost driver to be chosen. For the same reason that the optimized DirectFET gate connection reduces reliance on a high-strength gate driver, low impedance in the gate-drive circuit is also desirable. Using a low Rg MOSFET allows designers to match the impedance of the gate-driver output circuit with the impedance of the MOSFET gate circuit to ensure reliable, consistent switching when using a low-cost, low-power gate driver.

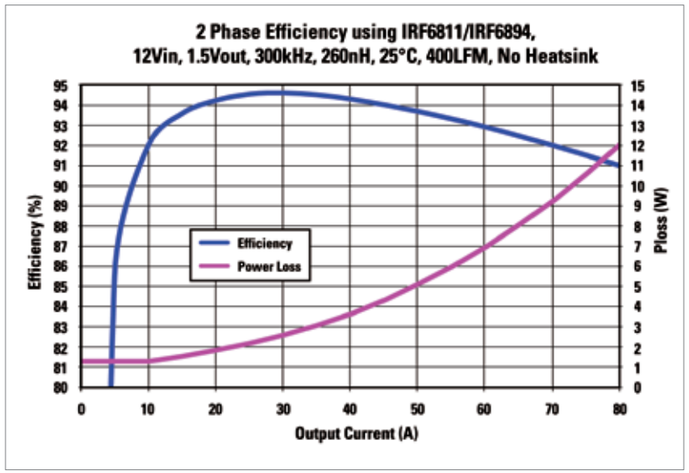

Figure 6: Performance potential of DirectFET plus family

Further Sync FET Optimization

During sync FET turn-on, the MOSFET body diode carries most of the load current in the period before the gate voltage has reached its threshold. When the gate voltage reaches its threshold, the load current gradually transitions into the MOSFET channel. Integrating a Schottky diode with the MOSFET die effectively minimizes the diode's reverse-recovery losses during this transition, thereby contributing to improved efficiency. The efficiency gains achieved by using a sync FET with integrated Schottky diode are greater at higher operating frequencies. This can be illustrated mathematically using the expression for power loss below, which shows how the influence of Qrr and diode conduction losses increases with operating frequency:

$$P_{loss} = (1-D)\bullet(I_{rms}^2\bullet R_{DS(On)}) + (Q_g\bullet V_g\bullet f) + (Q_{oss}\bullet V_{in}\bullet f)/2 + (Q_{rr}\bullet V_{in}\bullet f) + (t_{DT}\bullet I_{out}\bullet f \bullet V_f)$$

Device Design and Evolution

As far as device design is concerned, MOSFET Rg can be reduced significantly below 1Ω with no disadvantage in terms of other loss-related parameters.

When selecting MOSFETs for high-frequency synchronous rectifiers, engineers also now need to consider the effects of Rg on converter efficiency, in addition to the conventional $R_{DS(on)}$ x Qg FOM. Figure 5 charts the evolution of IR's DirectFET power MOSFETs in terms of the established FOM and the revised metric [$R_{DS(on)}$ x Qg x Rg]. The product is proposed as a new FOM to guide the design of high-frequency synchronous converters in the future.

Combined Strengths

The efficiency advantages of low Rg MOSFET is amplified further when combined with DirectFET package technology. Since a higher Rg tends to mitigate the switching speed advantages resulting from DirectFET's low gate inductance, a MOSFET with low Rg (less than 0.5Ω) will switch at high speed with lower gate drive when packaged in a DirectFET compared to an alternative such as PQFN. This can save engineers from having to specify a very strong driver, thereby enabling cost and power savings.

IR has combined these technologies in its latest DirectFET plus family of MOSFETs, enabling power supply designers to continue increasing the efficiency of synchronous converters for use in consumer and professional equipment spanning a variety of power ratings.

Figure 6 shows the efficiency achieved using a two-phase synchronous converter built using the IRF6811/IRF6894 DirectFET plus chipset. The 12V to 1.5V converter achieves peak efficiency of 94.5% when operated at 300kHz with no heatsink, showing how designers can achieve new standards of efficiency for power supplies in the 100W range.

Author: Omar Hassen, Executive Director and Vijay Viswanathan, Technical Marketing Manager International Rectifier

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POWER MANAGEMENT PURITY

BUS SIGNAL INTEGRITY AND NOISE REJECTION UTILITIES

By Frank Kern

Modern power systems feature high speed serial communication between load and voltage regulators (VR) to enable sophisticated power management operations. This communication is susceptible to environmental noise coupling that can corrupt digital transmission. In the worst case, noise corruption can break synchronization between clock and data, resulting in regular data transmission errors.

Some failure modes are periodic and can lead to repetitive communication errors that lock-up the bus even after the channel is reset. This can have a negative effect on the functionality or performance of the system powered by the voltage regulator. In computer systems, communication failures can result in 'blue-screening' or system lock up.

The bottom line is that noise is always present, whether from phase node coupling, cross-talk from neighboring transmission lines, ringing, or superposition of noise sources. The challenge is to guarantee good noise immunity that avoids data transmission errors. Application of transmission line theory and good layout practices are the standard methods of minimizing noise generation.

However, noise is not predictable, so failure to detect a noise generator may force a board spin when analog VR controllers are used. Analog circuits require a quiet layout to avoid noise corruption. They do not have the intelligence to distinguish noise from the digital signal they are trying to receive. By contrast, digital filtering uses intelligence to distinguish data from noise, thereby providing superior noise immunity in noisy power management bus designs. Designers can optimize powerful digital filter parameters in noisy environments to restore reliable data communication, thereby removing schedule risk and cost of undesirable board spins.

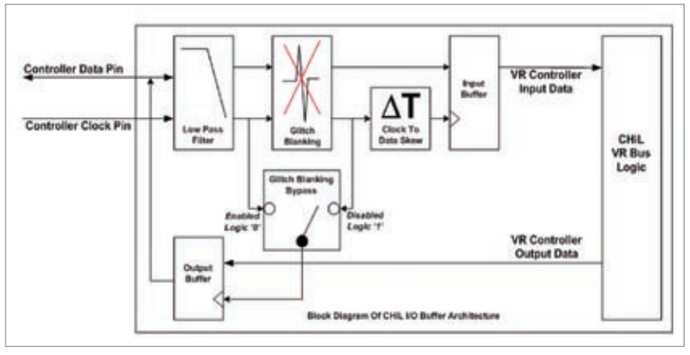

Figure 1: Noise Rejection Utilities

How is this done? One way is through the use of noise rejection utilities that repair high speed data communication failures. An example is controllers made by CHiL, which feature a digital control engine configured by a user-defined program stored in VR memory. Prior to power on, the noise rejection utilities can be programmed to aggressively filter noise. Programming is accomplished using CHiL's Intuitive Power Designer software, a companion to CHiL's VR controller chip. During validation, the filter settings can be further configured to achieve the optimal system response.

What causes noise corruption?
An incorrect exchange of data between master and slave is defined as a communication failure. Communication failures may occur when noise superimposed with the power management waveforms results in an invalid crossing of the receiving agent's input logic threshold voltage; this is known as noise corruption. Noise corruption is separated into two categories, data signal corruption and clock signal corruption.

Data signal corruption may occur if noise violates the input threshold voltage at the receiving agent's data pin during the setup/hold window. In these cases, the error can be flagged by the parity bit and a resend of the data has the potential to correct bad communication.

Clock signal corruption can lead to the most severe communication failure – loss of synchronization between clock and data, resulting in repetitive transaction errors. This occurs when a noise glitch crosses the clock's input voltage threshold and is detected by the receiving device as a valid signal. When this occurs, the data associated with the clock signal is latched into the receiving device twice – once by the noise glitch and once by the true clock signal. As a result, the data input of the receiving device is no longer synchronized with the clock; all future reads and replies are off synch by the number of detected noise glitches. The corrupted data pattern is read as an incorrect reply by the bus master or as an incorrect instruction by the bus slave.

Eventually, the bus master will detect incorrect replies and attempt to reset the bus. However, as noted above, it is likely that a noisy environment will repetitively disrupt communication causing regular performance degradation of load operations.

What are the noise rejection utilities?
CHiL adopts three utilities for noise immunity: low pass filters, glitch blanking utilities, and a variable clock to data line skew. Each utility features user programmable settings that require no external components. The utilities are configurable on the fly using CHiL Intuitive Power Designer software, and take less than five minutes to optimize. This eliminates hours of debug that might otherwise be required, thereby reducing the risk of board spins, and ultimately speeding time to market. Figure 1 shows a general block diagram of the noise rejection utilities.

The low pass filter is in series with the signal trace and the buffer input for both clock and data nets. This feature allows the VR designer to filter out high frequency noise associated with pulse ringing, crosstalk, and phase node coupling. The variable cut-off frequency reduces intermittent coupling from neighboring fields.

Table 1 – CHiL Default Noise Rejection Utility Variable Values

Parameter	Value
Low pass filter	113.7MHz
Glitch blanking utility	2.4 nanoseconds (ns)
Glitch blanking bypass	Off
Variable Clock Skew	0 nanoseconds (ns)
Bus timeout value	Application Dependent

Table 1 provides default noise rejection utility variable values.

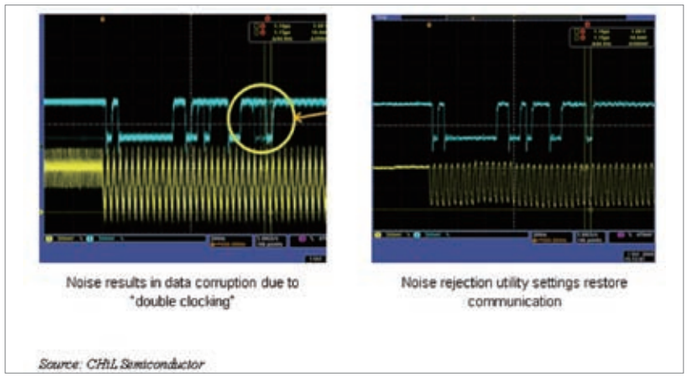

Figure 2: Noise Injection Experiment Results

It offers significant attenuation of coupled phase noise with a standard 20dB per decade roll-off.

The glitch blanking circuitry is also in series with the signal line and the buffer input for both clock and data nets. The receiver ignores pulse widths shorter than a programmable value. This circuit is configurable to 'blank' or ignore noise-related glitches that appear as artificial data or clock pulses. The receiver rejects threshold violations from crosstalk, pulse reflections, and coupled phase node noise. To minimize the impact to the controller's time from clock to output (Tco) specification, the clock signal path can be configured to bypass the glitch blanking circuitry.

The variable clock skew variable introduces a programmable skew (delay) between the clock and data at the VR receiver input, providing additional hold time at the cost of setup time. This is effective for shifting the setup/hold time window away from periodic noise.

When noise corruption disrupts data transfer, the bus master will traditionally reset communication by stopping the clock. The bus timeout value variable allows the VR designer to program the timeout duration based on specific application requirements. The bus master is a CPU, GPU, or validation tool that controls the bus operation and transmits the clock.

Digital noise rejection utilities ensure robust and error free communication in noisy environments

Adoption of digital utilities enables the industry's strongest noise tolerance, providing superior noise margin across all manufacturing variables. Runt pulses due to transmission line reflections are ignored using the glitch blanking utility. Noise coupled from the phase node is attenuated by the low pass filter and rejected by the glitch blanking utility. Ringing from trace inductances is attenuated using the low pass filter and rejected by the glitch blanking circuit. Runt pulses resulting from cross-talk are ignored using the glitch blanking utility. In addition, the setup/hold time window can be shifted to avoid periodic noise using the variable line skew.

The most impressive feature of the digital noise rejection utilities is an immediate reaction. Enabling the utilities results in immediate noise rejection, versus a 2-month design cycle spent correcting issues with a board spin. Greater noise immunity and reduction of the chance of intermittent issues gives designers higher confidence of a reliable design.

Noise injection experiments demonstrate effective repair of the communication channel

To verify reliability and robustness of the noise rejection utilities, CHiL conducted experiments in which noise was injected onto a high speed bus clock. The communication integrity was then observed with utilities turned off and compared to those enabled with optimal settings.

The experiment used two separate boards; one for the device under test (DUT) and one for the bus master. High speed signals between the bus master and DUT were connected using long fly-wires. The clock fly wire was wrapped in multiple loops and placed close to an inductor to enable noise pick-up. A 10-amp load was then drawn through a target phase (40 board at 10-amp/phase) resulting in fields that coupled periodic phase noise onto the clock signal.

In this configuration, CHiL researchers verified noise corruption on the communication channel. Coupled noise exceeding 0.5V regularly crossed receiver input threshold levels. With the utilities turned off, the VR controller intermittently 'rejected' or 'not acknowledged' communication – which verified communication errors. The experiment was then repeated under a variety of conditions with the noise rejection utilities turned on and properly tuned. The VR controller reliably 'acknowledged' each transmission packets without error. Data communication was found to be 100 percent% reliable in this noise polluted environment with utilities enabled and tuned.

Figure 2 illustrates the results of the noise injection experiments. On the left, noise resulted in regular data corruption due to "double clocking." Repetitive commands are sent across the high speed bus with the scope triggered on the clock waveform. The circled waveform (in infinite persistence mode) shows intermittent "acknowledge" replies, mixed with "not acknowledge" and signal "reject" responses. The blue trace is the data waveform and yellow trace is the clock signal. On the right, the low pass filter is set to 114MHz and the glitch blanking pulse width is set to 2.4ns. Intermittent 'not acknowledge' and 'reject' replies are no longer encountered and communications is fully restored without detection of any error.

The bottom line for designers is that application of transmission line theory and good layout practices are not always sufficient to avoid noise failures. Addition of CHiL's digital filtering is a designer's best option for ensuring reliable communication in noisy power designs. The outcome is reduced debug time and much faster time to market.

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Special Report: Energy Efficiency

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Power Systems Design: Empowering Global Innovation

Inside:

HIGH EFFICIENCY TUNING

Making better choices to optimize inductor selection

By Len Crane

Optimizing a power converter means making the right inductor choice. Choosing an inductor is a fairly simple proposition, with relatively few parameters to consider. Yet a solid understanding of key inductor properties and specifications is necessary to achieve new levels of power efficiency without sacrificing other attributes. Here we discuss the implications of two key parameters: DCR and saturation current.

In order to select an inductor it is necessary to consider specifications for both the average and the peak inductor current, as well as the difference between them. For example, a low voltage continuous mode buck converter is likely to have a large dc current with fairly small ripple, with a small difference between the peak current and the average current. Conversely the peak-to-average ratio in a discontinuous mode converter can be much greater. Since one inductor will not fit all situations, the designer must have access to properly detailed specifications to make the right choice for the application. Optimizing for DCR implies optimizing the design for the average current, whereas Isat means optimizing for the peak current. This leads to an important question: which balance is correct – better DCR or better Isat? For continuous operation of low voltage buck converters, the DCR is likely to be most important, whereas an emphasis on Isat may be more appropriate for situations like discontinuous mode and over current conditions.

DCR

There are some subtleties to dealing with this seemingly simple parameter. The DCR is most generally used as a measure of conduction loss, as described by $P = I^2R$. But let's take a look at the components of this equation. The 'I' is the time-averaged current. Buck regulator current is likely to have a substantial dc component with a fairly small triangular shaped ripple current, in which case the average current is the rms value of this waveform, a value somewhere between the dc value and the peak of the triangle. For discontinuous current topologies the average current is proportional to the on time.

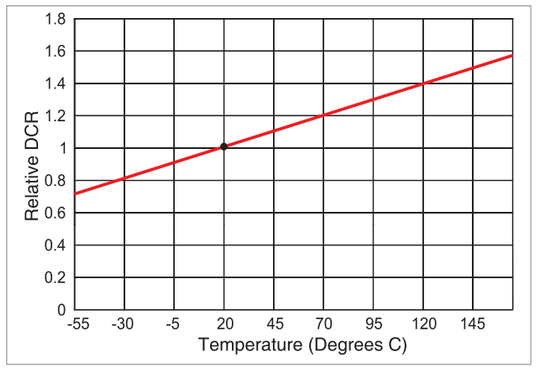

Figure 1

The second part of the power equation, the DCR, seems straightforward – not particularly sensitive to measurement techniques, not frequency dependent, etc. However there are a couple things to consider. First, while DCR is not frequency dependent, it does have a temperature dependency based on the wire type. For typical annealed copper wire, the temperature dependence is quite linear and the temperature coefficient of resistance is about .00393 per°C and the relative resistance at any temperature T can be calculated compared to the resistance at 20° C according to: $DCR = DCR_{20}[1 + .00393(T-20)]$[1] . From this equation a derating curve for DCR [figure 1] can be constructed for any inductor with copper windings. A useful rule of thumb is to remember the DCR will change about 10% for every 15°C.

Second, consider the effective DCR, that is, the DCR of the inductor in situ when soldered on a PCB, which may be higher than the DCR of the data sheet due to solder joint resistance. This is true for any soldered component, but especially significant for current carrying power path components. Solder joints can add significant fractions of milliOhms to the series resistance of the power path. Considering 2x solder joint resistance per inductor, along with the resistance of PCB traces, at some point there will be diminishing returns to further lowering inductor DCR. Lower DCR will still help marginally improve power efficiency, but once this point is reached, the designer might do well to consider focusing elsewhere for larger gains.

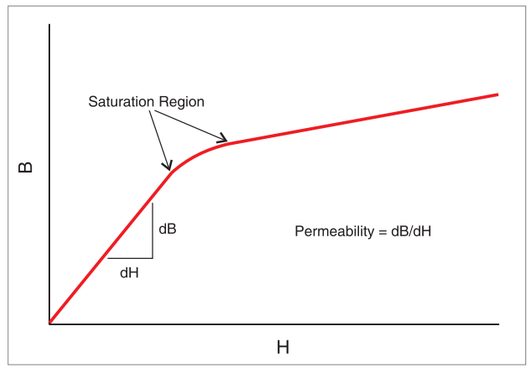

Figure 2

Why not simply look for the part with the absolute lowest DCR available? After all, even a small improvement in efficiency, is still an improvement. Even so, there is a cost. Optimizing DCR too far means a corresponding drop in Isat. These two key parameters are not directly connected but the properties that affect DCR often create design limitations for Isat and vice versa. Increasing the conductor (winding wire) diameter lowers DCR without affecting Isat. However, within a given inductor size, space is quickly used up and alternative means must be used for further DCR improvement. This can be accomplished by reducing the winding length through either a smaller number of turns or a smaller length per turn (core cross-sectional area). Both turn count and core cross-sectional area are inversely proportional to flux density; $\Delta B = (E\Delta T \times 10^8)/NA$, therefore reducing DCR by decreasing either the number of turns or core area causes the core to reach saturation flux density at lower current and reduces the Isat rating of the inductor. A significant part of the design task is to strike the right balance between optimizing for DCR versus optimizing for Isat.

Isat

Isat considerations start with how saturation is defined. It is convenient to define saturation as a percent drop in the inductance. For example, a 10% inductance drop definition is very conservative and insures very little inductance variation from zero current to the Isat rating. It is also common to see inductance defined by a 20% or 30% inductance drop, which is helpful if the design can tolerate a wider range of inductance.

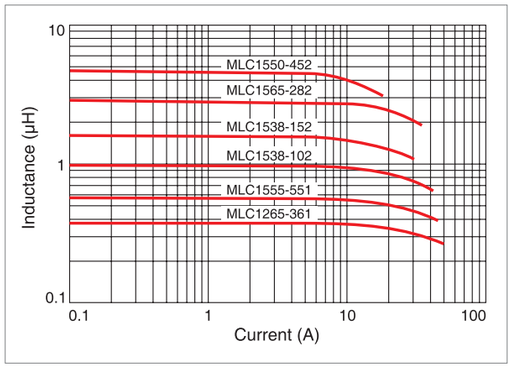

Figure 3

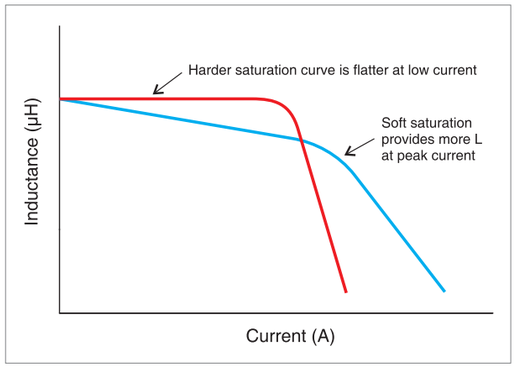

Figure 4

This simple definition of inductor saturation is quite useful for part to part comparisons, but since Isat rating is directly related to inductor size, operating farther along the saturation curve allows selection of a physically smaller inductor. Therefore more information is necessary to select the inductor that best optimizes both size and performance.

Consider the physical nature of the inductance drop caused by saturation.

Core permeability, and inductance, are proportional to the slope of the B-H curve, so when current (αH) becomes large enough, the flux density reaches the saturation flux limit of the core (Bsat), the incremental slope of the B-H curve decreases, and so does the inductance. The important thing to note for selecting an inductor is that permeability and inductance do not drop instantly to zero as Bsat is reached. The bend in the B-H curve is a region, not a single point

It can be seen from this discussion that Isat listed on a data sheet is primarily informational and should not be regarded as a fixed rating or limit. In fact, exceeding the saturation limit of a power inductor causes no damage to the inductor. Establishing a number for Isat allows meaningful comparisons, but too often that number becomes a de facto limit that designers are hesitant to exceed.

Since saturation is not completely described by a single point definition, the designer should refer to L-I curves to get the most complete understanding of the saturation characteristic. Curves for a typical power inductor family [figure 3] show a more complete picture of the L vs I characteristic over a wide range of current.

Different core materials, core shape, and air gap all have an effect on the shape of the saturation curve, so inductors with the same Isat "rating" may in fact have quite different saturating characteristics. Some inductors saturate quickly and others saturate more "softly". Softer saturation provides more inductance at the peak current at the expense of inductance stability at lower currents. Figure 4 demonstrates in more detail the possible differences between different inductor styles.

Summary

It is to be expected that a variety of inductor types are needed to meet the needs of present and future power converter applications. Optimizing for any particular parameter ultimately leads to a compromise of another. Understanding the key inductor parameters of DCR and Isat in greater depth enables the designer to make the selection that best suits the size and performance needs of each application.

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SECONDARY THERMAL PROTECTION

Preventing thermal-runaway damage in automotive and industrial power systems

By Guillemette Paour

The growing demand for electronics that can operate in harsh environments such as under-hood automotive systems and rugged industrial applications is fueling a trend toward new materials and more efficient power components.

High-power, high-temperature applications place greater demands on power electronic systems, resulting in the potential for serious thermal issues when components such as power Field Effect Transistors (powerFETs), capacitors, resistors or integrated circuits (ICs) fail due to long-term exposure to harsh environments.

Improving power component performance, using design techniques that spread heat more evenly, and incorporating new heat sink materials are some of the solutions that have been proposed to enhance thermal management. Nevertheless, many designers currently rely on secondary protection to help stop thermal runaway events that can be generated by power component failures or corrosion-induced heating.

The most common approach is to use a thermal fuse/Thermal Cut Off (TCO) or a thermal switch. These devices both offer the designer wide and specific temperature activation characteristics in both AC and DC applications, but they present challenges in the board assembly process. Because more and more printed circuit boards (PCBs) utilize only surface mount components, using a through-hole device can translate to special mounting procedures and additional cost and complexity. Additionally, standard devices may not provide the ruggedness and reliability needed for automotive

applications; whereas components that are qualified for the automotive environment are fully tested to meet stringent shock and vibration specifications and provide the proper DC ratings.

In response to the need for a robust, reliable surface mount device that can help prevent thermal damage resulting from

failed power electronics, Tyco Electronics recently introduced the Reflowable Thermal Protection (RTP) device. The secondary thermal protection device can be used to replace redundant powerFETs, relays and heavy heat sinks typically used in automotive and industrial electronic designs.

PowerFET failure in harsh environments

In the harsh automotive environment, powerFETs are routinely subjected to extreme temperature variations and thermo-mechanical stress. Intermittent shorts, cold operating environments, high arcing or noisy short circuits, as well as inductive loads and multiple short circuits can, over time, fatigue the device and cause it to fail in open, short or resistive mode.

Although powerFETs are increasingly robust, they are prone to failures which can occur very quickly if their ratings are exceeded. If the maximum operating voltage of a powerFET is exceeded, it goes into avalanche breakdown. If the energy contained in the transient overvoltage is above the rated avalanche energy level, the device will fail; causing a destructive thermal event that may result in smoking, flame or desoldering.

Automotive powerFETs have been shown to be more prone to fatigue and failure than devices that are installed in less demanding applications. When comparing powerFET failure rates over time, devices used in harsh environments, such as automotive applications, exhibit greater ppm failure rates. After five years in the field the difference can be more than a factor of ten.

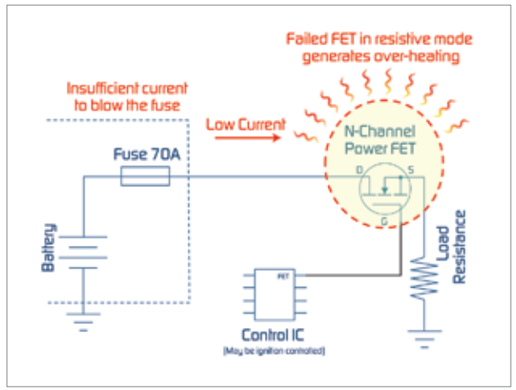

Figure 1: PowerFET failure in resistive mode can lead to unsafe overtemperature conditions

Although a powerFET may pass initial testing, it has been demonstrated that, given certain conditions, random weak points in the device can result in field failure. Even in situations where the powerFET is functioning within specified operating conditions, random and unpredictable resistive shorts at varying resistance values have been reported. The resistive mode failure is of particular concern, not only for the powerFET but for the PCB. As little as 10W may generate a localized hot spot of more than 180°C, well above the typical PCB's glass transition temperature of 135°C, damaging the board's epoxy structure and leading to a thermal event.

Figure 1 describes a scenario where a failed powerFET may not generate a hard short overcurrent condition but instead, a resistive short which produces unsafe temperatures through I^2R heating. In this case the resulting current may not be high enough to blow a standard fuse and stop thermal runaway on the PCB.

Reflowable thermal protection solution

If a power component failure or a board defect generates unsafe overtemperature conditions the RTP device, which opens at 200°C (a value above normal operating temperatures but below lead (Pb)-free solder reflow temperatures), will interrupt the current and help prevent a thermal runaway condition that may lead to critical damage.

As shown in Figure 2, when the RTP device is placed in series on the power line in close proximity to the FET, it tracks the FET temperature and opens the circuit before a slow thermal runaway condition can generate an undesirable thermal condition on the board.

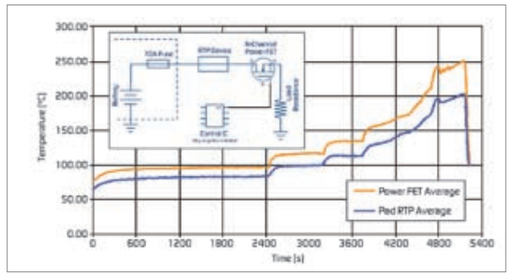

Figure 2: In a slow thermal runaway condition, the RTP200 device tracks the powerFET temperature until it opens the circuit at 200°C

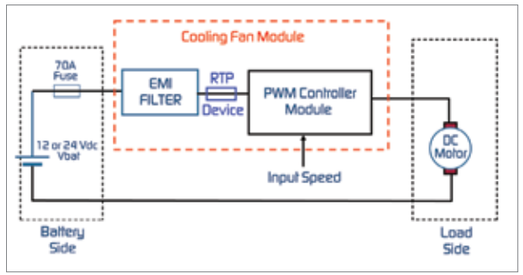

Figure 3: Block diagram of RTP device placement in CFM application

Protecting cooling fan modules from damage caused by thermal runaway

Cooling fan modules (CFMs) are an essential element of the vehicle's HVAC and engine cooling systems, helping to cool the engine and prevent potential overheating under specific conditions, such as hot weather and steep hill driving. Figure 3 shows placement of the RTP device in a CFM application. CFM modules are typically placed under the hood and they experience more extreme temperature variations than those found in the passenger compartment. This thermal stress can accelerate fatigue of the powerFET and lead to early failure. Under-the-hood components may also be exposed to "fluid attacks" leading to corrosion and localized hot spots on the PCB.

Typically, CFMs do not include a micro-controller which, under certain conditions, could be used for onboard diagnostics and automatic initiation of the turn-off signal to the powerFET. As a result, a software approach to preventing powerFET failure is not available, and secondary protection is needed so that thermal runaway does not cause a dangerous thermal event.

How it works

The RTP device's 200°C open temperature helps prevent false activations and improves system reliability since it is a value above the normal operating window of most normally functioning electronics, but below the melting point of typical Pb-free solders. As a result, the device will not open if surrounding components are operating in their target temperature range, but it will open before a component de-solders and creates the potential risk of additional short circuits.

To allow it to open at 200°C in the field, the RTP device utilizes a one-time electronic arming procedure to become thermally sensitive. Before arming, it can withstand three Pb-free solder reflow steps without opening. Timing of electronic arming is user-determined, and can be implemented to occur automatically at system power up or during system testing.

Summary

The RTP device helps protect against thermal-runaway damage caused by failed FETs, capacitors, ICs, resistors and other power components that can crack or corrode. The device's thermal sensitivity is beneficial since, in some cases, failed power components may not generate a dead short circuit overcurrent condition, but instead may create a resistive short that cannot be opened by a traditional fuse. This type of event may actually reduce load current, but can still result in thermal runaway conditions. The RTP device helps prevent damage caused by both dead short circuit and resistive short circuit conditions.

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POWERING FLEXIBILITY AND RELIABILITY

Digital power conversion with improved current sharing

By Andrew Skinner

Flexibility is one of the major advantages of power supplies using digital power conversion, where customer specific optimisations can be achieved without the expense of changing the hardware. Andrew Skinner, Chief Technology Officer of TDK-Lambda UK explains how current sharing power supplies operating in parallel can be improved significantly without compromising reliability.

Power supplies with digital control are gaining in popularity. However the term 'digital control' is commonly applied to two quite different meanings. 'Digital power management' where customers communicate with the power supply to monitor status and adjust certain parameters remotely such as voltage, current limit, etc. and 'Digital power conversion', which is still in its infancy in terms of products available commercially, involving replacement of the common power supply analogue control loop with a digital control loop.

Figure 1: The effects of parallel connecting two power supplies without share control

When two or more power supplies are connected in parallel, the power supply with the highest output voltage will supply the load; the second unit only supplying current when the output voltage of the first falls below the voltage of the second. The amount of load required to achieve some degree of sharing is dependent on the setting accuracy, load regulation and thermal drift of the supplies used. For power supplies with a small variation in output voltage with load, no sharing may occur until the first power supply is overloaded and enters current limit - see Fig. 1.

The normal solution to this problem is to have a separate circuit that forces current sharing. This usually takes the form of a single wire connection between all the power supplies that are paralleled known as a current share bus. The bus effectively acts as a current demand reference and all the power supplies endeavour to follow this. In theory, this is quite a good solution since it maintains good load regulation but in practice at light loads it doesn't tend to work very well; it is not uncommon to require a minimum load for sharing to occur. The current share bus is also a single point of failure for the whole system since loss of the bus could result in zero demand to all the power supplies. Now one of the main reasons for paralleling power supplies is to improve reliability by having an N+1 setup – so to have something where you have a single failure point bringing the system down completely defeats the objective.

Another less common solution to provide sharing between paralleled power supplies is to increase the load regulation (the amount the output voltage changes with load). By doing so, the output voltage changes more quickly with load current and therefore not as much current is needed in the higher voltage power supply before the lower voltage one starts to carry current (see Fig. 2). In this scheme there is no share bus and hence no single point of failure. In a number of high reliability applications, including some telecom systems and a number of medical applications, this is the preferred method of current sharing. This method is often referred to as 'droop sharing'.

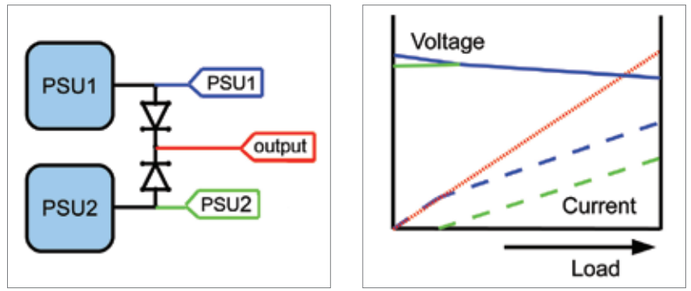

Figure 2: Characteristics of parallel connected power supplies incorporating droop share

Clearly there are some applications that require droop but many applications with only one power supply that don't. On the EFE series, which uses digital power conversion, the normal setting for a single power supply unit is just as you would expect with a nominally zero slope. However, for paralleling, rather than having a fixed output characteristic, which you would find in most power supplies, on the EFE series the load regulation is defined as one of the many programmable features. Effectively this feature allows the 50% load point voltage to be set -5/+10% of nominal and the load regulation can be programmed with either a positive or negative slope. The control algorithm is programmed such that the result of the slope is always within the specified output range.

Optimising the power supply performance in this way has become possible due to TDK-Lambda's strategic decision to develop its own digital power conversion intellectual property from scratch rather than use some of the proprietary devices now available. Engineers need to fully understand the algorithms involved in order to maximise the flexibility that digital power conversion can bring.

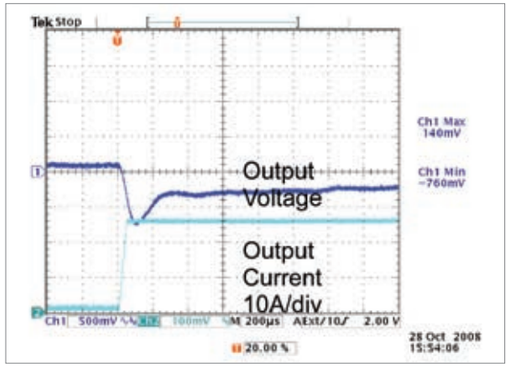

Figure 3: Application of 0-100% load transient to EFE300-12 at 90Vac with no additional output capacitance

Referring back to Fig.1, if the two power supplies are operated in parallel with no droop sharing then for most load conditions, one carries all of the current (and consequently runs hot) and the other one sits there doing nothing (consequently running cooler). In itself, this does not cause a problem other than the fact that reliability and life are temperature-dependent. However, some topologies when lightly loaded will enter a different operating mode (e.g. PWM controlled forward converters will go into discontinuous-mode resulting in a high effective output impedance until the control circuit recovers resulting in a low output voltage if fully loaded). If PSU1 fails then the duty-cycle of PSU2 must ramp up from its very low level in order to supply the load before the output capacitor discharges. This could require significant additional capacitance to be fitted in order for the combined output to stay within acceptable limits.

Conversely the EFE300M, which includes an ORing MOSFET, operates in a way in that ensures the correct output voltage is maintained even at zero loads and that the output impedance remains at a low level. Droop , when specified, will improve current sharing and product life but, even when droop is not specified redundancy will still be achieved due to the excellent 0-100% load-transient performance of the EFE, see Fig. 3.

Andrew Skinner concluded that the beauty of digital power conversion in supplies such as the EFE range is that customer specific droop characteristics are simple software changes with standard hardware thus reducing cost, speeding up time to market, and improving overall system reliability.

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DESIGNING FOR EFFICIENCY

Driving AC-DC power supply efficiency ever higher

By Peter Blyth

Reducing the size and improving the efficiency of AC-DC power supplies are constant pressures. In addition, the requirement for portability in some equipment means that not only the size but also the weight is a prime consideration in the selection of power supplies.

A designer can always find a smaller power supply, or design one, by including a fan to provide forced air-cooling. This might save one-third to one half of the total volume of a typical unit in this way. However, in the medical market the main disadvantage of this approach is fan noise, which disturbs and irritates patients. Other problems include a significant reduction in reliability – the fan will likely be the only moving part in the power supply, and you add a maintenance problem. Due to these issues, system designers are now looking to utilize convection-cooled power supplies to power their equipment.

Minimizing component-count will help in reducing size and cost, but you will be limited here too. This means you can't tolerate compromises with respect to immunity to interference (EMC/EMI/RFI) and production of conducted or radiated emissions. You can't compromise safety either – users have to be fully protected from potentially lethal voltages. Finally, you need to take account of green legislation including RoHS, CEC/EISA, particularly if equipment is going

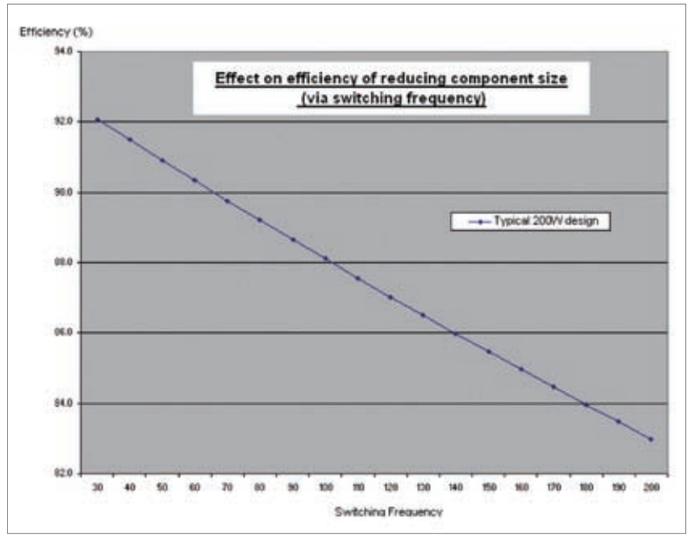

Figure 1: Effect on efficiency of reducing component size by increasing switching frequency

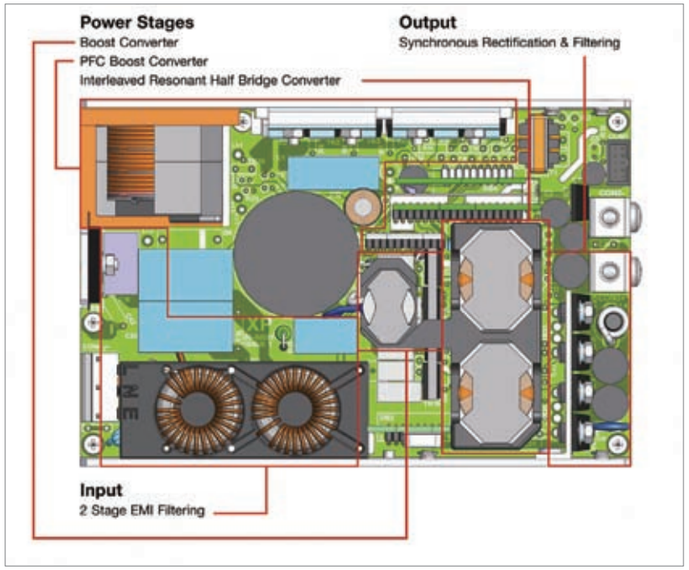

Figure 2: This 250W AC/DC power supply is up to 95% efficient

to be sold around the world.

Reducing power supply size without compromising performance means that you have to work towards incremental improvements in every aspect of the design, both electrical and mechanical.

The size - power - efficiency trade-off

The surface area available to provide cooling will be the limiting factor in how much heat you can dissipate from a convection-cooled power supply – one that doesn' t need a fan. It follows that the more efficient you make the power supply, the less heat you'll need to remove and the smaller the unit can be. What may appear to be small differences, can have great impact here. If you can buy or design a power supply that is 95% efficient, versus one that's 90% efficient, the 5% difference in efficiency means you need to remove less than half of the heat of the less efficient design. For a 250 Watt power supply, this means 14.6 Watts less heat to be dissipated.

Incidentally, because power supplies for portable equipment might be used in a lot of different environments, you cannot always rely on a 230V or 110VAC power source being available. It's important to look at how well the efficiency is maintained across the range of input voltages defined in the power supply data sheet, particularly at low line (85-90VAC). Some units are very much worse than others.

Efficiency will also be affected by load – most power supplies operate at maximum efficiency at full rated load. It pays to check out the efficiency you can expect in your individual application.

One way to reduce the size of magnetic components and capacitors is to increase the switching frequency of the converter. However, switching losses increase with frequency due to wound component core losses and increased copper/resistive losses caused, in part, by skin effect. The trade-off for efficiency and switching frequency in a typical 200 Watt power supply produced during the last few years is shown in Figure 1.

Clearly, you have to reach a compromise between size, efficiency, switching frequency, reliability, lifetime, cooling technique and, perhaps most importantly, the cost for a given power rating.

Designing for 90%+ efficiency

The best of today's 250 Watt, convection-cooled power supplies operate at over 90% efficiency across an input voltage range of 90 to 240VAC. This level of efficiency is essential in order to keep within an industry-standard 6 x 4 inch footprint whilst still ensuring adequate heat dissipation without a cooling fan or large external heatsinks.

Over 90% efficiency can only be achieved with near lossless switching in the active power factor correction circuit, the main converter(s) and the rectifiers. A diagram for a 250 Watt AC/DC power supply that achieves up to 95% efficiency at 240VAC input and 92% efficiency at 90VAC input is shown in Figure 2.

From the outset achieving high efficiency was the primary design goal for this power supply. Consequently, for each stage the power loss budget was determined and this drove the choice of circuit topology. Power losses were minimized in each stage, striving to save every mW of unnecessary dissipation. For example the input filter for the power supply shown above uses very low resistance winding wire that virtually eliminates I^2R losses in the chokes.

The EMI filter employed in this design is a 2-stage filter with a high permeability magnetic core. This was carefully selected to attenuate switching noise and to minimize power loss. The other components in the filter are X and Y capacitors with the Y capacitor values being chosen so as not to exceed 300uA of earth leakage current, as set out in UL60601-1, the most widely referenced medical standard.

A quasi-resonant, lossless power factor correction circuit operates in a discontinuous mode. Its operating frequency changes between 30kHz and 500kHz to achieve zero current switching (ZCS) throughout the specified range of loads and input voltages. This is important because it ensures that the voltage switches when the current is truly at zero, thereby eliminating switching losses.

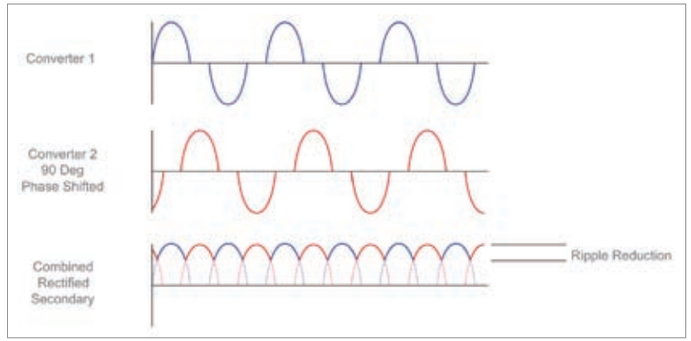

Figure 3: Combining the outputs of two converters that are 90-degrees out of phase reduces ripple level and doubles ripple frequency

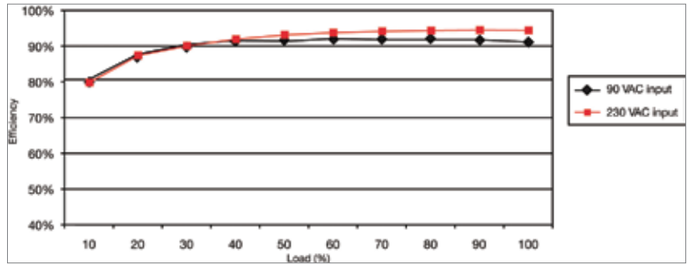

Figure 4: ZCS switching and the use of resonant converters delivers high efficiency over a wide range of loads and input voltages, not just at full load

The main converters are of fixed frequency, resonant, half-bridge design – again with lossless ZCS. Two transformers are employed; the combination has lower I^2R switching loss than if one larger transformer had been utilized. The two converters operate at 51.2kHz and one of them has its output phase-shifted by 90-degrees. Combining the outputs reduces ripple and doubles the ripple frequency, as illustrated in Figure 3. In turn, this halves the value, and size, of the output filter capacitors.

A feedback loop monitors the power supply output and varies the boost converter voltage, which in turn varies the voltage at the input to the main converters. The primary purpose of the boost converter is to boost the PFC voltage of approximately 380Vdc to 420Vdc. This enables the design of the main converters to be optimized around tightly defined voltage parameters, another factor that helps to achieve high efficiency. The final stage uses synchronous rectification instead of normal diodes as this greatly reduces power loss.

Timing for the boost converter, main converters and synchronous rectifiers needs to be precisely controlled to achieve accurate ZCS. A crystal-controlled clock is used as the timing reference and a divider network is employed to get the desired switching frequency. Using this approach is crucial for the efficient operation of synchronous rectifiers, especially for higher output voltages.

This power supply architecture results in high efficiency across a wide range of loads and input voltages, as Figure 4 demonstrates.

A further benefit of ZCS is the relatively low levels of both conducted and radiated emissions as well as the output ripple and noise. The power supply referred to above exhibits less than 90mV peak-to-peak ripple and noise at 20MHz bandwidth and is below the level B limit line for EN55011 for conducted and radiated emissions. Creative mechanical design minimizes size and improves thermal performance.

You can greatly improve the thermal performance of a power supply through creative mechanical design. Avoiding hot spots and ensuring the best possible air-flow around components that are going to get hot are both important.

Combining the best of proven design technologies with creative mechanical design has led recently to the introduction of units that can reach up to 95% efficiency, a figure thought impossible only a few years ago. Further incremental improvements are going to be harder to achieve, but the decades of experience that many engineers now have in power supply design, coupled with advances in semiconductor technology, will make them possible.

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COMFORT WITH CONSERVATION

Latest reverse conduction IGBT technology for air-conditioning systems

By Thomas Kimmer and Mark Thomas

The demand for energy in our world is increasing dramatically. A large portion of this demand comes from air-conditioning systems that are running over all the different climate zones. Energy saving can be optimized using variable frequency drives with the best cost and performance-optimized power electronics.

Increasing demand of power electronics for inverterized drives

The demand for these systems is increasing resulting in a usage of high efficient systems that can only be realized with the utilization of modern power semiconductor devices. The increasing demand on power electronics is driven by strong factors that are not only based on end-customer requirements in electricity saving, but also programs of governments emphasize the usage of advanced solutions for the compressor and the fans in air-conditioning-systems. Power electronics usage is a common trend in washing machines, fridges, freezers and dryers basically effecting a wide range of the so called white-goods applications that are benefiting from the usage of frequency variable drives. Trends are set by the white good producers that implement drives and inverters that can bring their systems energy consumption down to fulfill the requirements set by energy efficiency classes that go beyond the commonly known classes like A++. Differentiation in the market is done with new strategies that quote top-runner models of the year or systems that are 40% more efficient than the A group are

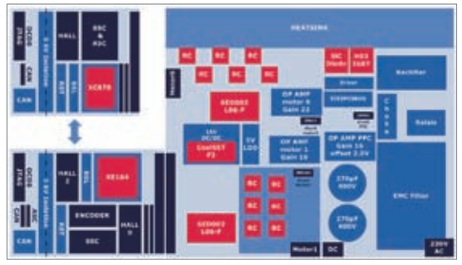

Figure 1: Application reference design for air-conditioning systems.

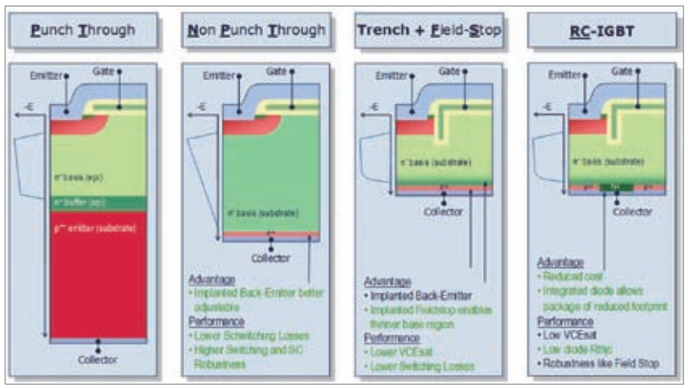

Figure 2: Vertical structure of IGBTs as a generation evolution.

labeled with "A-40 per cent".

Infineon offers a wide portfolio of energy saving chips for the whole system chain of power electronic devices for air-conditioning systems. To enable engineers a fast entry in the usage of our devices we developed a reference design that controls the compressor and the fan with minimized bill of material to achieve an efficient and powerful control for air-conditioning system shown in Fig. 1. The reference design is split into an inverter section and a control section realized on two separate printed circuit boards. This enables the user to interchange different controllers and adopt existing control solutions.

The reference design uses the industry standard field orientated control with a single-shut solution to lower the energy consumption and increase the comfort functions. In air-conditioning systems the usage of induction machines is quite common, but they are usually running with a constant speed. Inefficient mechanical switching stages are used since they are simple and easy to implement. The usage of permanent magnet synchronous machines is not only resulting in a size reduction of the system they are also resulting in a silent operation and an increase of efficiency.

Innovative semiconductors for air-conditioning systems

A recent trend is the application specific usage of power electronic devices in the form of discrete products. In the last years more and more modules where established in the motor-inverters, due to the simplified design in procedure and the production simplification. Due to a multiple sourcing strategy and a flexibility in selection of the different semiconductor sections the trend now goes in the opposite direction enabling cost saving potentials with discrete devices. Microcontrollers, drivers and power semiconductors can be arranged in the wanted configuration. But not only the selection of the best fitting devices is an issue also the thermal design and the production facilities have to be taken into account.
To help our customers with this process the "Air-Conditioning Inverter Kit" was released to guides engineers to realize a price optimized system. On a single PCB a compressor up to 1.2kW and a fan (200W) can be controlled. The board can run on the 110V and the 230V grid and offers with the microcontroller board the two motor-inverter and the PFC.ds with an 8-Bit controller (XC-878) that is capable of controlling PFC and a single motor and the 16-Bit controller (XE-164) for controlling two motors and the PFC.

In air-conditioning inverters a B6-full bridge configuration is used where the IGBT is the most preferred power semiconductors since it has all the preferences on a high power density and a good commutation behavior of the anti-parallel diode. The most recent IGBT TRENCHSTOP™ technology now replaces conventional non-punch trough und punch-trough IGBTs in all frequency classes and offers an extremely performant usage in terms of overall power losses, EMC behavior and cost effectiveness.

Usually the IGBTs used in inverter systems are using a freewheeling diode that is integrated in a duo-pack solution using two dies in a single package. Infineon's new RC-drives technology has this diode chip monolithically integrated in the IGBT structure itself (Fig. 2).

The monolithically integration enables a shrink of the common duo-chip solution up to 40%. This enables the usage if smaller packages for the same current class. A typical TO-220 or TO-263 (D^2-PAK) can be replaced with the next smaller ones TO-251 (I-PAK) or TO-252 (D-PAK). Leading to a smaller footprint on the PCB and resulting in cost- and space-saving. The reference design uses 15A devices for the compressor and 4 A for the fan both SMD mounted devices. Usually frequencies between 5kHz and 16kHz are used for these inverter stages since it's always a sacrifice of performance to go for higher switching frequencies for the compressor 5 kHz are used and for the fan 16kHz if these inverters are used in an living environment the switching frequency for the compressor can be increased according to the audible noise limit with power limitations. The RC-drives technology offers very low conduction losses (Vcesat) and still low switching losses (Ets) with a very soft turn-on turn-off behavior to low the EMC.

The latest Highspeed 3 generation brings the IGBT technology to the high speed switching world in power factor correction systems. The economic attractive replacement of planar MOSFETs with IGBTs enables further cost saving potentials and makes the decision easier to use an active PFC in the system. In combination

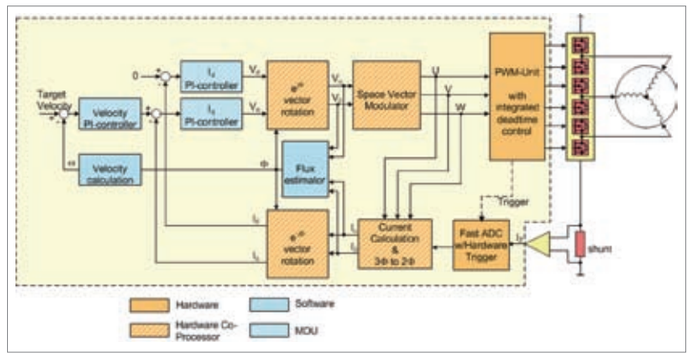

Figure 3: Block diagram of the field oriented control used in the air-conditioning system.

with the latest SiC-Diodes in the ThinQ!-technology efficiencies of above 97% can be achieved with conventional 67 kHz boost PFC systems. If the usage of lower switching frequencies is preferred e.g. 40kHz standard Si-based diodes can be the right choice these power diodes based on Infineon's emitter-controlled again lower the cost for the power devices but also increase the size of the passive components. The PFC function on the board is realized in two ways a PFC IC (ICE3PCS02G) is on the board that can quickly provide the functionality if further functions are needed the PFC function can be provided by the microcontroller.

Optimized control algorithms

For established open-loop control of the synchronous machines trapezoidal or block commutation with the usage of hall-elements or back EMF sensing causes noise especially at low speed and additionally limits the maximal speed. The field oriented control (FOC) leads to overall system efficiency due to sinusoidal currents with a low torque ripple and a wide speed range (Fig. 3). For a quick start a full tool-chain is included in the evaluation kit. The field-oriented control is implemented for both inverters using a single-shunt based feedback loop.

Thermal Concepts for air-conditioning systems

The removal of the dissipation loss of power semiconductors is a key issue in the system design. If through-hole-technology (THT) is used, the removal of the dissipation loss can be realized relatively easy. For the THT profile heat-sinks are used, which are isolated by heat conducting film from the IGBT and which are clipped to the components. The heat transfer for this technology is very efficient, whereat the technical production costs are immense. An alternative to the THT components is the use of surface-mounted devices (SMD), they are generally easy to integrate into the production process and do not require manual intervention. The power semiconductors can be contacted to the heat-sink

through various methods. Neat solutions for contacting is the use of IMS-materials (Insulated Metal Substrates), for which aluminum is used as a thermal interface material, which offers significantly better thermal conductivity than the standard FR4 material. In the area of white goods, these materials are not very common due to higher costs. For a good heat dissipation of SMD packages Infineon recommends the usage of two-layer FR4 PCBs with thermal vias. A good thermal coupling of the IGBT lead frame to the heat-sink is achieved when using 200µm thick vias. These will be nearly closed during the manufacturing process of the circuit board through the copper electrolysis and offer a good alternative to pure copper inlays. The vias can be distributed across the IGBT leadframe surface because solder is no longer pulled away from the SMD package. Conditions of manufacture of larger vias are also possible; Infineon recommends an array of vias outside of the lead frame. The isolated compound of the PCB to the heat sink is possible over a wide range of self adhesive heat conducting foils.

Conclusions and outlook

Newest power semiconductor technologies enable high efficiencies for air-conditioning inverters at reduced system costs. The usage of small SMD D-PAKs in inverter topologies above 1kW opens new horizons for power density increase. New IGBTs are currently under development that will allow the usage of these devices for all power ranges at frequencies above 16kHz to increase the comfort function of the inverters. In combination with powerful microcontrollers and driver ICs the bill-of-material can be reduced significantly and make the system reliable and cost efficient.

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EFFICIENCY COST & COMPACTNESS

GreenChip fixed frequency flyback controller

By Yingying Wang

The current market of Switch Mode Power Supply IC's shows increasing demand on efficient and cost effective solutions that enable slim and compact design. The industry standard Energy Star Version 2.0 requires the external power supplies to have average active mode efficiency higher than 87% and no load standby power lower than 300mW (output power <50W), or 500mW (output power from 50W to 250W).

Many customers actually have even more demanding requirements such as standby power less than 100mW. With the GreenChip TEA1733 flyback controller, 90% efficiency and less than 100mW standby power can be simultaneously obtained with minimum amount of external components. A 65W/19.5V demo board for notebook adapter is shown in Figure 1. The TEA1733 is suitable for almost all applications with power requirement up to 75W. Typical applications include netbook adapters, LCD monitors and printer adapters. This controller can be used in Discontinuous Conduction Mode (DCM) as well as Continuous Conduction Mode (CCM). The combination of fixed frequency operation at high output power and frequency reduction at low output power provides high efficiency over the total load range. Frequency jitter is implemented to reduce electromagnetic interference (EMI). The IC is also equipped with several protections to enhance robustness and reliability.

Figure 1: 65W demo board of the TEA1733 Fixed frequency flyback converter

A flyback converter is the most

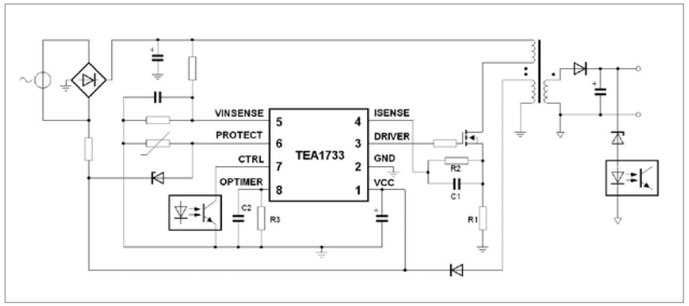

Figure 2: Typical configuration of the TEA1733

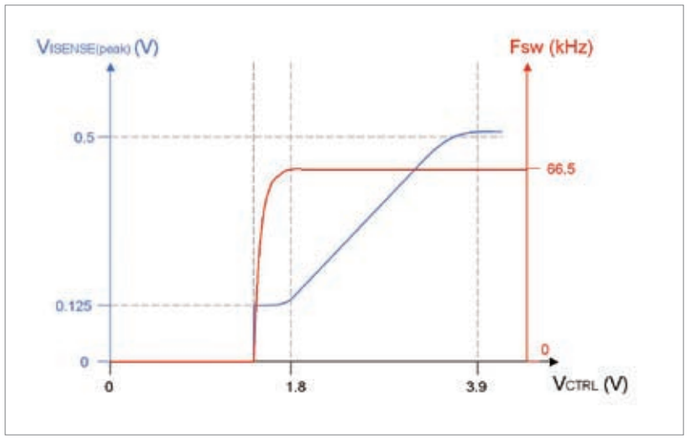

Figure 3: ISENSE peak voltage and switching frequency as a function of CTRL voltage

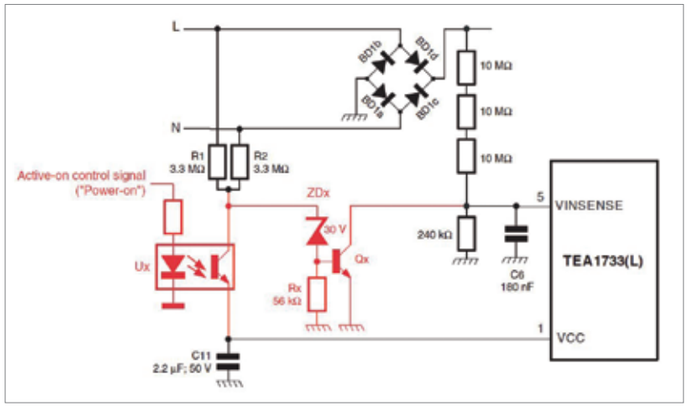

Figure 4: "Zero Watt" application with active-off signal

ubiquitous switched mode power supply topology today. The typical configuration of the TEA1733 in a flyback topology is shown in Figure 2. The TEA1733 uses peak current control and the output power is regulated by the CTRL pin. The load is measured and transferred back to the CTRL pin via an optocoupler. The primary current across an external resistor R1 is sensed through the ISENSE pin. Its peak is compared and adjusted with an internal voltage, which is proportional to the CTRL voltage. By controlling the peak current, the duty cycle is adjusted accordingly. When the duty cycle is above 50%, slope compensation is activated to avoid sub-harmonic distortion. The maximum duty cycle is limited at 74%.

In low power operation the switching losses are reduced by lowering the switching frequency. An internal Voltage Controlled Oscillator (VCO) reduces the frequency gradually down to 0Hz. To prevent audible noise, the peak current is set to 25% of the maximum peak current as the frequency reduces. The frequency and peak current control curves can be found in Figure 3.

The TEA1733 integrates frequency jitter in order to reduce EMI emission. The center frequency of 66.5kHz is smeared over +/- 4kHz by a jitter oscillator. The frequency of the jitter oscillator is chosen to be 260Hz to avoid the audible noise.

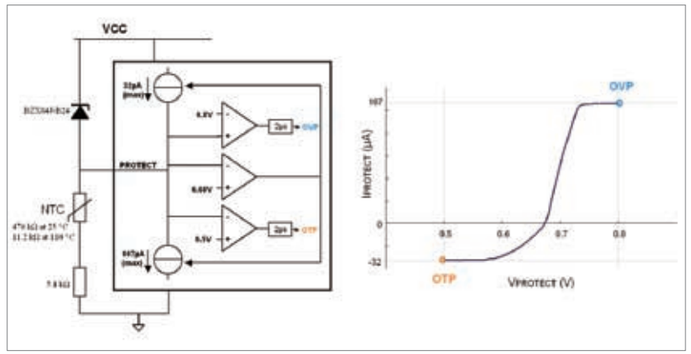

Figure 5: Block diagram and the VI curve of pin PROTECT

During start-up, the supply voltage VCC is charged by the current through a start-up resistor, and the current consumption of the IC is only around 10µA. No high voltage start-up circuit is required. As soon as VCC reaches its start-up level of about 20.6V, and all the other conditions are met, the controller starts to switch. From that moment on, the supply voltage is taken over by the auxiliary winding of the transformer. The normal operating current is typically 0.5mA excluding load at the DRIVER pin. The low current consumption helps to increase the efficiency.

Standby operation

Because of the low current consumption and frequency reduction, a standby power of less than 100mW can be achieved by using TEA1733. With proper choice of external components such as resistors and the X-cap, the measured standby power is 48mW at 115VAC and 84mW at 230VAC for a typical 65W, 19.5V power supply.

If there is an external "Power on/down" signal available to indicate the standby mode, like the battery operated equipment, the standby power can be further reduced to below 30mW by switching off the entire application. This is referred to as "Zero Watt" design. The basic application diagram of "active off" situation is shown in Figure 4, in which the external "Power-down" signal turns high during the standby mode. Then Transistor Qx conducts and pulls down the VINSENSE voltage, which initiates the restart protection. The IC immediately stops switching and enters power-down mode. In the power-down mode, the IC consumes only 10µA current. In the meantime, VCC is clamped to just below the start-up level to guarantee a quick restart after a standby situation.

Protections

TEA1733 features various protections, for instance, Input Over-Voltage/Under-Voltage Protection, Output Over-Voltage Protection, Over-Power Protection, and internal/external Over-Temperature Protection. The above protections lead to either safe restart or latched protection. For safe restart protection, the IC goes into power-down mode first, and wakes up when all the conditions are satisfied. In the power-down mode the OPTIMER pin is quickly charged to 4.5V and then slowly discharged to 1.2V. In a latched protection, the IC also goes into power-down mode, but the VCC voltage is clamped to around 6V. In order to reset the latched protection, the VCC voltage has to go below a certain level by unplugging the mains. The 6V clamp is just above that level to enables fast reset after a latched protection.

A special function of TEA1733 is that the PROTECT pin can realize two protections: external Over-Temperature Protection and Output Over-Voltage Protection, as illustrated in Figure 5. The PROTECT pin has the current source capability of 32µA and sink capability of 107µA. The internal circuit tries to regulate the PROTECT pin to 0.68V. No protection will be set if the PROTECT voltage is between 0.5V to 0.8V. If the VCC is so high that the maximum sink current is not able to pull the PROTECT voltage below 0.8V, Output Over-Voltage is detected. This protection can be used with general purpose. With increasing temperature, the resistance of the negative temperature coefficient (NTC) thermistor connected at the PROTECT pin decreases. If

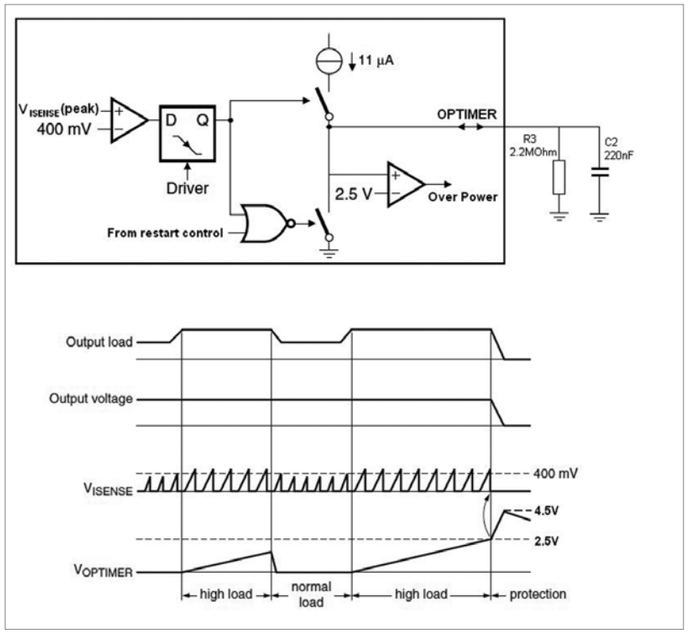

Figure 6: Block diagram and the waveforms of over power time-out

the maximum source current is insufficient to keep the PROTECT voltage above 0.5V, external Over-Temperature is detected. Both situations lead to the latched protection.

Adjustable over power time-out

Temporary over load situation is allowed if the OPTIMER pin is connected as Figure 6. When ISENSE peak voltage is above 400mV, 11µA current flows out of the OPTIMER pin to charge the external capacitor C2 and the over power timer starts. For long over load situation, the Over-Power Protection is activated as soon as the OPTIEMR voltage exceeds 2.5V. For short over load situation, if the ISENSE peak voltage drops below 400mV before the OPTIMER voltage reaches 2.5V, C2 will be immediately discharged and no protection will happen. The over power time can be adjusted by choosing different values of C2 and R3.

High/low line compensation

In fixed frequency CCM the maximum output power depends not only on the primary peak current but also on the duty cycle and therefore the input voltage. The TEA1733 has built-in input voltage compensation to ensure accurate Over-Power Protection that is nearly constant over the full mains. The over-power compensation circuit measures the mains voltage via the VINSENSE pin, and converts it to a current flowing out of the ISENSE pin. This current generates a voltage across the soft start resistor R2 in Figure 2, which limits the maximum current through the sense resistor R1. By proper tuning of R2, the maximum output power becomes independent of the input voltage.

Available versions

The TEA1733 has several versions to meet the requirement of different applications. The standard version causes safe restart for over power time-out. The TEA1733L triggers latched protection for over power time-out. Derivatives operating at 90kHz are available in a safe restart version as TEA1733A and a latched protection version as TEA1733M. Besides SO8 package, the TEA1733(L) IC is also available in DIP8 package, known as TEA1733(L)P.

Conclusion

The TEA1733 has become the first product in the complete new GreenChip series of lower power AC-to-DC control IC's launched by NXP Semiconductors. Its high level of integration makes it possible to fulfill the growing demand on low cost and compact power supply designs. Less than 30mW standby power is achieved with "Zero Watt" design. The power performance especially at standby mode distinguishes it from other controllers for low-power computing and communication applications.

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EMERGING APPLICATIONS NEED ENERGY-SAVING DESIGN SKILLS MOST

By David G. Morrison

Power electronics (PE) engineers have long been concerned with improving the efficiency of the power supplies and power systems they design. But now, with energy efficiency being a pressing concern for society as a whole, the role of the power electronics engineer in designing efficient power supplies and power systems takes on added importance.

Although the significance of this role may not yet be recognized by the general public, within certain industries, the power electronics engineer's energy-saving skills are especially valued. To gauge where power electronics engineers may see the greatest demand for their design skills as a result of energy efficiency requirements, I asked several executives in the power supply and power semiconductor industries to assess which applications or industries have the greatest demands for energy efficiency and where these demands translate into the most, potentially lucrative opportunities for power electronics engineers.

Here are some of their responses. While these answers do not represent a comprehensive survey of the industry, the consensus among these suppliers regarding certain industry trends may help PE engineers to understand how requirements for energy efficiency in emerging applications may translate into career opportunities now and in the future.

Efficiency is Critical For Data Centers and Consumer Products

Which applications have the greatest demand for energy efficiency? Among the industry executives I queried, the most-frequent response was data centers and/or their servers. One power supply industry analyst, Mohan Mankikar of Micro-Tech Consultants, asserted that the major effort to improve energy efficiency concerns this application area. Mankikar pointed to several factors that are driving demand for higher energy efficiency in this area. "Data centers are energy/power hogs," said Mankikar "so even a slight increase in efficiency means big savings."

Mankikar also noted that governmental mandates for energy efficiency and the actions of server manufacturers are other reasons energy efficiency is so important. The U.S. government, through the Environmental Protection Agency (EPA), "has mandated these energy savings for government servers and data centers, which are being expanded into private servers and data centers," said Mankikar. "Meanwhile, server manufacturers such as HP, SUN, IBM, Intel, Google, etc. have taken an active role in creating this energy efficiency environment."

Within the power semiconductor industry, suppliers of energy-saving silicon carbide (SiC) and gallium nitride (GaN) power devices also cited data centers and servers as a key market demanding energy efficiency. Alex Lidow, CEO of Efficient Power Conversion (EPC), a supplier of the new GaN power transistors, placed servers and routers atop his list of application areas requiring energy efficiency.

"Servers/routers have received a lot of attention due to the high cost of running server farms coupled with the demand for more and more farms. This concentration of cost has elevated the server energy consumption (MIPS/watt) to one of the key design criteria for server manufacturers," said Lidow.

Portable and consumer electronics was another application area frequently cited as having great demand for energy efficiency. "The power draw is quite small, particularly in standby, but because there are hundreds of millions of devices being deployed (laptop power supplies, phone and camera chargers, and LCD TVs), the overall energy usage is considerable," said Mankikar who explained that "the state and utility companies are driving the push toward more-energy efficient products, because the average consumer is not that concerned—an extra 20 W per hour will not register much on an electricity bill."

Solar Power Demands PE Engineers For Efficiency
So if servers and portable electronics are among the applications with the greatest requirements for energy efficiency, are these the industries where power electronics engineers can have the greatest impact and where their skills will be in greatest demand? Not necessarily.

Original equipment manufacturers in both of these industries have tended to outsource power supply design as discussed here in previous columns. That outsourcing pushes the design of ac-dc power supplies and adapters to power supply manufacturers, and the design of dc-dc converters to IC manufacturers, who provide chipset solutions, reference designs, and even completely customized dc-dc converter designs.

Although demands for energy efficiency may impact requirements for power electronics expertise in the power semiconductor and power supply industries, these are mature industries that serve a wide range of applications with a wide range of requirements that include but are not limited to high efficiency. In other words, the connection between requirements for energy efficiency and opportunities for power electronics engineers is a little less clear.

So where does demand for high energy efficiency appear to translate into the greatest need for skilled power electronics engineers? Dan Schwob, vice president of Sales and Marketing at SemiSouth Laboratories, a manufacturer of SiC products, pointed to solar power.

"The key industry that is absolutely focusing on energy efficiency is the solar market and in particular, solar inverters. There is a very high demand for power electronics engineers for the solar industry especially in Europe," said Schwob, who also noted that "after solar, both UPS and IT/telecom power supplies are also very much focused on improving efficiency."

Michael O'Neill, business development engineer for SiC Power Products at Cree, expressed a similar sentiment saying, "The two largest segments of business that we have that [pay] a premium for efficiency are in solar and server power supplies. Solar pays the premium for enabling the greatest possible energy harvesting from the panels."

Note that when Schwob and O'Neill refer to server power supply companies paying a premium for efficiency, they are speaking from the perspective of a component supplier since their companies provide the SiC Schottkys used in these applications. The perspective in the power supply industry may be different. David Norton, VP of marketing at TDK-Lambda Americas, explained that demands for efficiency translate into just a small premium for server power supplies.

EPC's Alex Lidow, a long-time advocate for energy efficiency within the power semiconductor industry, also noted the importance of solar and wind power in creating demands both for energy efficiency products and the power electronics engineers needed to design those products. When asked about the applications with the greatest demands for energy efficiency, Lidow noted six specific areas and ranked them roughly based on the size of their associated markets for power management devices:

1. Servers/Routers
2. Portable Electronics
3. White Goods
4. Alternative Energy Generation (Solar and Wind Power)
5. Lighting
6. Transportation

However, when asked which of these application areas represent the greatest opportunities for power electronics engineers, Lidow did not follow the above ranking.

"The two areas where a power management engineer can most directly affect the value of the end product and therefore command the highest salary in the long term) are #4 (alternative energy), and #6 (transportation) because these are emerging end markets that rely on efficient power management for their success," said Lidow.

"In all the other areas listed, power management will improve the performance of the system in measurable ways, but will only partially influence the success of the end product in the market. For example, you can sell a washing machine with a somewhat inefficient motor drive, but you cannot easily sell an inefficient solar panel or wind turbine. Similarly, an inefficient electric car will not help the transition from petrochemical-based vehicles to electric vehicles," said Lidow.

Another factor that makes being a PE engineer in these industries potentially lucrative is fact there are still many technical challenges to be solved in the applications. "These end markets are also immature technically," said Lidow, "so there is a lot of room for the power designer to innovate with new materials and topologies with corresponding opportunities for powerful intellectual property."

About the Author
David G. Morrison is the editor of How2Power.com, a site designed to speed your search for power supply design information. Morrison is also the editor of How2Power Today, a free monthly newsletter presenting design techniques for power conversion, new power components, and career opportunities in power electronics. Subscribe to the newsletter by visiting

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RENEWABLE SOURCES COMPETE

By Cliff Keys

In this issue themed on energy efficiency, it's good to get positive news on the new sources and the usage of this energy, but there will be challenges in the years ahead. Government stimulus funding worldwide, which helped finance many capital-intensive renewable installations, is being replaced by deficit cutting, which will reduce subsidies.

Governments argue that renewables policies were both correct and effective, as technologies have advanced, ecosystems of suppliers have developed, and costs have declined - approaching parity with fossil fuels.

According to a new report, Global Markets for Renewable Energy from BCC Research, the value of the global market for renewable energy is expected to increase to $331 billion in 2015, for a 5-year compound annual growth rate (CAGR) of 8.1%. The largest segment of the market, wind energy, is projected to increase at a CAGR of 6% to $87 billion in 2015, after being valued at an estimated $65 billion in 2010. Hydroelectric energy, is estimated at $62 billion in 2010, but expected to increase at a CAGR of 3.5% to reach nearly $74 billion in 2015. Solar energy will see the highest rate of growth in the next 5 years with a CAGR of 17.1%, rising from an estimated $44 billion in 2010 to $97 billion in 2015.

As prices for renewable energy sources get more competitive, suppliers will be forced to compete. Wind power will be required to lower prices, but solar power with its much larger customer and manufacturing base, will be able to respond more quickly.

Looks like an exciting era ahead.

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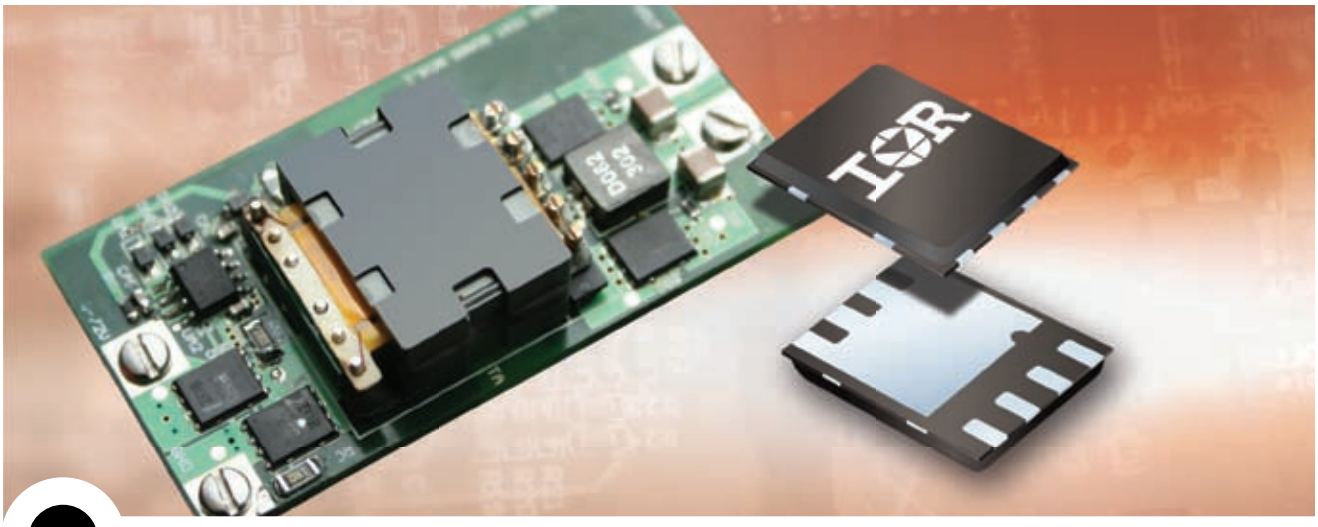

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IRFH5006TRPBF	PQFN 5x6mm	60 V	100A	4.1 mΩ	67 nC
IRFH5106TRPBF	PQFN 5x6mm	60 V	100A	5.6 mΩ	50 nC
IRFH5206TRPBF	PQFN 5x6mm	60 V	98A	6.7 mΩ	40 nC
IRFH5406TRPBF	PQFN 5x6mm	60 V	40A	14.4 mΩ	23 nC
IRFH5007TRPBF	PQFN 5x6mm	75 V	100A	5.9 mΩ	65 nC
IRFH5207TRPBF	PQFN 5x6mm	75 V	71A	9.6 mΩ	39 nC
IRFH5010TRPBF	PQFN 5x6mm	100 V	100A	9.0 mΩ	65 nC
IRFH5110TRPBF	PQFN 5x6mm	100 V	63A	12.4 mΩ	48 nC
IRFH5210TRPBF	PQFN 5x6mm	100 V	55A	14.9 mΩ	39 nC
IRFH5015TRPBF	PQFN 5x6mm	150 V	56A	31 mΩ	33 nC
IRFH5020TRPBF	PQFN 5x6mm	200 V	41A	59 mΩ	36 nC
IRFH5025TRPBF	PQFN 5x6mm	250 V	32A	100 mΩ	37 nC

Logic Level Gate Drive

Part Number	Package	Voltage	Current	$R_{DS(on)}$ Max. @4.5V	Q_G Typ @4.5V
IRLH5034TRPBF	PQFN 5x6mm	40 V	100A	2.4 mΩ	43 nC
IRLH5036TRPBF	PQFN 5x6mm	60 V	100A	4.4 mΩ	44 nC
IRLH5030TRPBF	PQFN 5x6mm	100 V	100A	9.0 mΩ	44 nC

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