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SPECIAL REPORT: RENEWABLE ENERGY (Pg 25)

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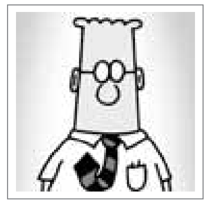

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AGS Media Group
146 Charles Street
Annapolis, MD 21401 USATel:
+410.295.0177
Fax: +510.217.3608
www.powersystemsdesign.com

Editorial Director & Editor-in-Chief
Cliff Keys
cliff.keys@powersystemsdesign.com

Contributing Editors
Liu Hong, Editor-in-Chief, Power Systems Design China
powersdc@126.com

Ash Sharma, IMS Research
Ash.sharma@imsresearch.com

Dr. Ray Ridley, Ridley Engineering
RRidley@ridleyengineerng.com

David Morrison, How2Power
david@how2power.com

Publishing Director
Jim Graham
jim.graham@powersystemsdesign.com

Publisher
Julia Stocks
Julia.stocks@powersystemsdesign.com

Circulation Management
Kathryn Phillips
Kathryn.phillips@powersystemsdesign.com

Research Director
Meghan Corneal
Meghan.corneal@powersystemsdesign.com

Magazine Design
Louis C. Geiger
louis@agencyofrecord.com

Production Manager
Leo Jiang
leow@action-new.net

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Volume 7, Issue 10

RENEWABLES AND REVENUES

Welcome to this issue of PSD where we present a special feature on renewable energy. The focus on renewables - and especially energy harvesting, has certainly hit the industry' s headlines over the past year. Apart from being good for the environment and good for the power electronics industry, it is a sought after lever for governments and administrations to attract 'clean votes'. With previous waves of engineering graduates trained in analog, logic and DSP technologies, maybe the next wave will be qualified as energy harvesting experts encompassing all of the above. It most likely hangs on the investment made now in education at this level, which probably depends heavily on the state of the economy and government priorities, to use a broad-brush term. Hopefully this relatively new industry will spawn the next wave of valuable and talented engineers who will take up and solve the real challenges facing our energy-hungry environment.

After nearly two years of unimpressive performance, the recovery of the global market for Uninterruptible Power Supplies (UPS) is picking up momentum. The industry on 3Q-2010 performed 12.9% higher than 3Q-2009, according to IMS Research. There were strong UPS sales in Asia and the Americas, while the debt crisis in Europe is still hampering its revival. China and India remain the engines of growth in Asia with a rapid uptake in shipments across all sectors. Without question, Asia is now a major focus of supplier attention. In the span of five years, Asia has grown its share of the global market from 25% to 33%. The market in Europe, Middle East and Africa has not improved to the degree of those in Asia and the Americas, where UPS revenues remain roughly the same as in 2009.

The rapid recovery in automotive production and inventory rebuilding among sensor component suppliers has set the market for automotive MEMS sensors to expand to record size in 2010, according to iSuppli. Marking a new high-point for the industry, shipments of automotive MEMS sensors will reach 662.3 million units in 2010, up 32.1% from 501.2 million units in 2009. The recovery in automotive MEMS shipments represents a turnaround from the depressed levels of 2009 when shipments reached a nadir, and the years ahead will provide additional room for expansion. One significant source for automotive MEMS growth is the use of sensors in passenger cars supporting mandated safety technologies such as electronic stability control (ESC) and tyre pressure monitoring systems (TPMS). The United States and Europe lead the adoption of legislation on such safety systems – with many other countries following suit.

I hope you enjoy this issue with the ongoing improvements to the magazine and website design based on your valuable feedback. And please check out Dilbert at the back of the magazine.

All the best,

Cliff
Editorial Director & Editor-in-Chief, Power Systems Design
Cliff.Keys@powersystemsdesign.com

INDUCTIVE COMPONENTS FOR RENEWABLES

The market for inverters for photovoltaic systems that feed solar energy into the electricity grid and for converters for wind turbines is experiencing strong growth. SMP has become one of the key global suppliers of magnetically soft materials for industrial applications, serving customers throughout the world.

SMP's chokes for inverters in wind turbines are now approved for use in offshore installations. These inductive components feature low losses, very low stray fields and a highly compact design. The chokes' cores consist of powder composites, which SMP has specifically engineered for this application.

The direct current from the wind turbines must be converted into a sinusoidal waveform with the values required by the grid. The converter's filters, which consist of capacitors and filter chokes, ensure that the current being fed into the grid exhibits a near sinusoidal waveform. To maximize the inverter's efficiency, its components must exhibit low losses. The materials that SMP developed especially for use in its energy-efficient, high-performance chokes have low magnetostriction and exceptionally low eddy current and hysteresis losses. Their encapsulated design ensures that the power converters emit only low-intensity stray fields, so that they do not affect other components. The chokes have a space-saving compact design, are maintenance-free and have a long lifespan – a significant contribution to cutting the maintenance costs for offshore wind turbines.

Offshore wind turbines are prone to corrosion. To protect them from the corrosive action of the sea water, special salt-resistant materials, additional corrosion protection and a complete encapsulation of certain subassemblies are necessary. SMP's inductive components for wind turbine inverters are now certified IP66 and approved for use in offshore installations. Because of their high protection class of IP66, these chokes can be fitted outside the inverters, which means that the heat generated by the choke is not discharged inside the inverter. This results in a lower internal inverter temperature, which removes the need for cooling fans, saving both energy and installation space. Placing the choke outside the inverter has the further advantage of reducing the inverter's overall dimensions, which further cuts space and energy demand. To simplify mounting outside the inverters, SMP provides the chokes with special mounting fixtures. The choke and the mounting plate are fitted on the device's outside and the connecting cables pass through a sealed opening.

SMP supplies inductive components for frequencies up to 200kHz and current ratings up to 1000A for use in onshore wind turbines, photovoltaic plants, railway engineering, medical engineering as well as in drives, power electronics, power generation, and instrumentation and control. Depending on their application, they are constructed either as single-conductor chokes for high-current applications, single-phase individual chokes, three-phase choke modules or LC filters. These components offer a high energy storage capacity in a compact and cost-conscious design as well as reduced losses and good EMC characteristics. SMP manufactures all components to customer specifications using in-house developed powder composites. All products are RoHS- and REACH-compliant and the materials used are UL-listed. To allow for a wide range of requirements, components can be made to all common international standards.

www.smp.de

CHALLENGES FOR RENEWABLE ENERGY

By Thomas Grasshoff

If we look back over the last 10 years, major changes have taken place in the market perception of power electronics. In the past, neither the public nor the press focused much on power electronics or the use of power electronics in motor, pump or elevator drives. With the boom of renewable energies, however, this has changed dramatically.

The onset of wind power generation was more than 20 years ago. SEMIKRON was already manufacturing intelligent power modules based on the new pressure contact technology and featuring integrated driver electronics, sensors and cooling unit – pre-tested and optimized systems.

Today, the onus is slightly different. In the fourth generation of SKiiP IPMs featuring integrated driver and heat sink, the main focuses are high power density and overall reliability. This is why every SKiiP module undergoes a 2-hour burn-in test under real 4Q inverter conditions before it leaves our premises.

Now, most wind turbines have an output of 2- 3MW. Work on the 5MW class has already begun, with initial offshore and mainland installations already in the test stages. The next step up to the 7.5 - 10MW class is under development. For power electronics this is a major challenge. Available space in the nacelle is limited but power is increasing. More compact and more efficient solutions are required. The SKiiP4 is the most powerful intelligent power module with an output power of 3600A on the market and is 33% more powerful than its predecessor SKiiP 3.The design was optimized to cope with high DC link voltages and high installation altitudes of up to 4500m above sea level.

There are two ways to reduce the costs of power electronics - either by reducing the thermal resistances between the junction of the chips and the environment or by increasing temperature towards operating temperatures at and above 150°C. Temperature increase has a major impact on module lifetime and new assembly technologies are the key to further improvements in this area. Solder melting temperatures of 250° C are too close to the maximum silicon operating temperatures and lead to delamination and ultimately module destruction. Sinter technology based on a thin silver interface with a melting temperature of 960°C prevents aging and reduces the thermal resistance by 20% compared to traditional solder joints.

In the area of thermal efficiency there is one major drawback: the thermal paste layer between the module and the heat sink has 400 times the thermal resistance of copper, is difficult to apply and is responsible for 60% of the thermal resistance between chip and heatsink. Module manufacturers are working on technologies to combat this "heat blocking paste problem" and are soon to deliver power electronic systems with improved thermal efficiency.

The solar inverter market faces slightly different challenges. Typical topologies used to achieve high inverter efficiency are HERIC or H5 circuits. At the moment, SiC is entering the market and providing an additional 1% efficiency gain. 3-level topologies, known from UPS or traction applications, are now being used in new designs for applications above 10kW. With 3-level inverters, the same efficiency as for SiC topologies can be achieved.

The more pressing call, however, is for greater reliability. If a 500kW solar inverter breaks down, the off-line time affects the business of the solar investor. A solar field operates under entirely different operating conditions: the difference between full sun exposure and shade are rather high. Inverter solutions with monitoring functions for current, temperature and voltages are needed. 3-level topology is currently also entering the market for solar applications of up to 250kW.

These two applications in the area of renewable energies underline the importance of power electronics when dealing with the challenges of energy generation and conversion. Technological developments will continue and make the electrification of other applications attractive too.

Author: Thomas Grasshoff
Head of Product Management
SEMIKRON INTERNATIONAL
Nuremberg, Germany

www.semikron.com

RENEWABLE ENERGY MARKETS CONTINUE TO SHINE

By Ash Sharma

Renewable energy is currently one of the most exciting sectors for power companies. This is particularly the case for solar power, not least because of the major market growth, but also because of changes in architecture and interesting market dynamics that present massive opportunities for power electronics manufacturers.

The solar (PV) power market continues to show incredible resilience and has captured the attention of many major component vendors. Despite one of the market's key generators of demand (Spain) collapsing in 2008, the overall market still achieved growth of more than 30% in 2009, amidst one of the worst economic environments in decades. In 2010, with most developing nations still recovering from the recession, the global PV market will more than double in size. Global installations are likely to exceed 16 GW (roughly the same as the four previous years combined) and solar power now provides 20% of market leader Germany's peak power requirements – quite an incredible feat.

To put this rapid industry growth in context, the total PV equipment industry generated revenues of more than $40 billion in 2010. If you included the construction, financing, design, and maintenance of installations and also the production equipment needed to make the components, this figure would be closer to $100 billion. The power electronics industry's share of this market is not insignificant either: DC-AC inverter revenues are likely to surpass $5.5 billion this year. Again, in context, this is larger than either the datacom or computing merchant power supply markets. Furthermore, although short-term fluctuations in demand are likely, the PV market is set to grow on average at more than 20% per year over the next five years. High growth aside, the solar industry presents a particularly attractive opportunity for power component vendors due to its appetite for high efficiency, high-value devices (e.g. Silicon Carbide diodes), its high power density requirements, and typically low pricing pressure, with suppliers often enjoying margins of close to 40%.

Although many inverter designs use discrete components, most of the industry's opportunity currently exists for high power IGBT module vendors. And whilst inverter volumes are still relatively low (a few million shipped this year), the emergence of micro inverters and DC-DC power optimizers presents a major new market for power semiconductor suppliers. These power conversion products are deployed on a per panel basis (typically around 200W), rather than on a per-string or per-plant basis used in traditional architectures. As such, potential volumes for these devices are orders of magnitude higher, making them very attractive to suppliers of devices like power ICs and MOSFETs. The outlook for the micro inverter and power optimizer market has improved considerably in recent months following announcements from several leading panel companies that they would be integrating these technologies directly into their panels. A year ago it appeared these new disruptive products would be limited to small-scale residential systems, but now they appear well placed to take centre stage.

Author: By Ash Sharma
Research Director
IMS Research
www.imsresearch.com

POWER SUPPLY DEVELOPMENT DIARY

Part IX

By Dr. Ray Ridley

This article continues the series in which Dr. Ridley documents the processes involved in taking a power supply from the initial design to the full-power prototype. In Part IX, the second-generation of the PC board is described, and a critical area of layout is detailed.

Second Generation PCB

A second generation PCB was designed to accommodate errors in layout of the first pass board. This second design incorporated changes to component sizes where needed, and changes to the power supply specification. As described in the previous article of this series [1], a decision was made to attempt to provide four regulated outputs with a single supply after it was discovered that the real output power needed by the load was less than anticipated. This resulted in a major change to the magnetics, and testing of this concept was not possible on the first revision of the circuit board.

At each pass of the printed circuit board, the design should be made as complete as possible in order to move as close as possible to a production PCB. With major changes such as those encountered in this design, it is reasonable to anticipate as many as four iterations of the board design. The second iteration, shown in Figure 1, has many significant changes, and there may be some design issues to be tested and fixed with a further iteration.

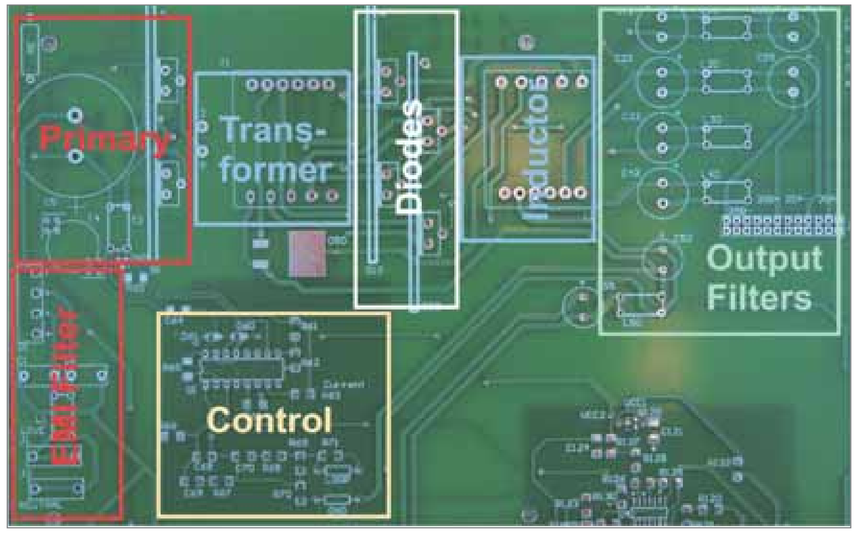

Figure 1: Second-pass PC Board Design

Figure 1 shows the bare PCB with the major areas of the power supply. EMI filters are included on this board design, located close to the power entry and shown in red. The primary circuitry, also outlined in red, comprises the main input filter capacitor, and the two primary switches and clamp diodes. The power transformer and power inductor are shown outlined in blue. The new iteration of the power board has five outputs, using a coupled inductor. The layout of this region of the converter is particularly challenging, and will be described in a future article.

The control circuit is outlined in green in Figure 1. Bias power is supplied from an auxiliary power supply, and there is no direct connection between the control circuit and the primary of the power circuit.

A ground plane is located under the area of the control circuitry to provide quiet operation. More details of how ground and power planes can be used to improve the PCB layout for power supplies will be given in upcoming articles.

Control Chip Layout – Critical Timing Capacitor Location

There is a common problem with the layout of power supply control chips, one that I see in many designs. Conventional PWM controllers use a current source to charge a capacitor, and then use the resulting ramp for the PWM modulator. The clock pin of these types of control chips is usually a very noise-sensitive part of the circuit.

It is crucial that the timing capacitor for the ramp be placed as close as possible to the PWM controller, and connected with very short traces to the pins of the chip. Figure 2 shows a circuit layout that did not work well. While the timing capacitor (on the bottom layer of the board) is close to the pins, the ground connection to the chip is too long. This resulted in significant noise on the clock, and the measurements of power supply transfer functions were severely affected by this noise. Some of the noise problems that can be exhibited by the clock are described in [2].

For this example, the long ground connection resulted from breaks in the ground plane, not from an intentional routing. This was overlooked in the first review of the board design.

Layout with Noise Problems

The importance of this part of the control circuit layout is paramount. In some cases, improper layout of this timing capacitor will directly lead to failure of the power supply. I have encountered this many times in my design career. The failure mechanism sometimes results from the clock working at very high frequencies during high-current operation, leading to overstress and failure of the power switch.

Layout with Moved Timing Capacitor

Figure 3 shows a proper way to lay out this part of the circuit. The timing capacitor, shown in red, is located on the bottom of the circuit board, and connected with very short traces to the pins. With this arrangement, there are no clock noise problems, and control performance is very predictable and accurate.

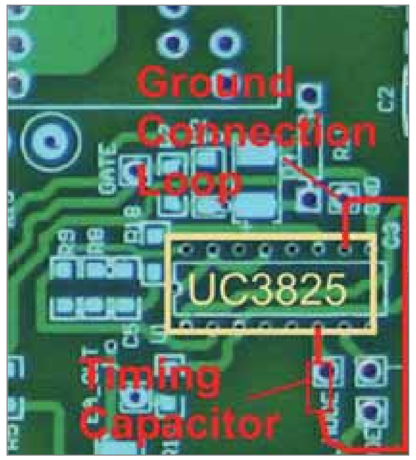

Figure 3: Detail of Control Chip

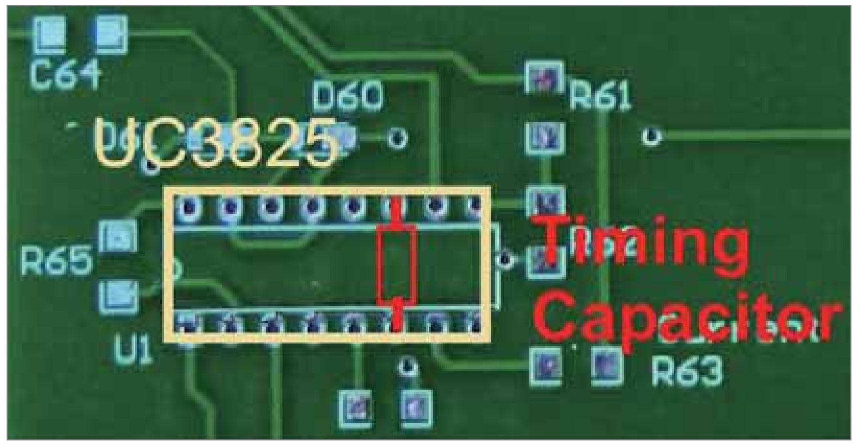

Figure 2: Detail of Control Chip

Summary

Small details of PCB design can make or break a power supply. In this article, the detail of the layout of the timing capacitor is described. This is often the most crucial layout detail of the entire power supply. In following design tips article, other critical considerations for the board layout design will be described.

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1. "Power Supply Development Diary Parts 1-VIII", Ray Ridley, Power Systems Design Magazine, 2010.
2. "Six Reasons for Power Supply Instability", Ray Ridley, Switching Power Magazine. www.switchingpowermagazine.com.

Author: Dr. Ray Ridley
President
Ridley Engineering
www.ridleyengineering.com

THE PROMISE OF SOLAR TECHNOLOGY

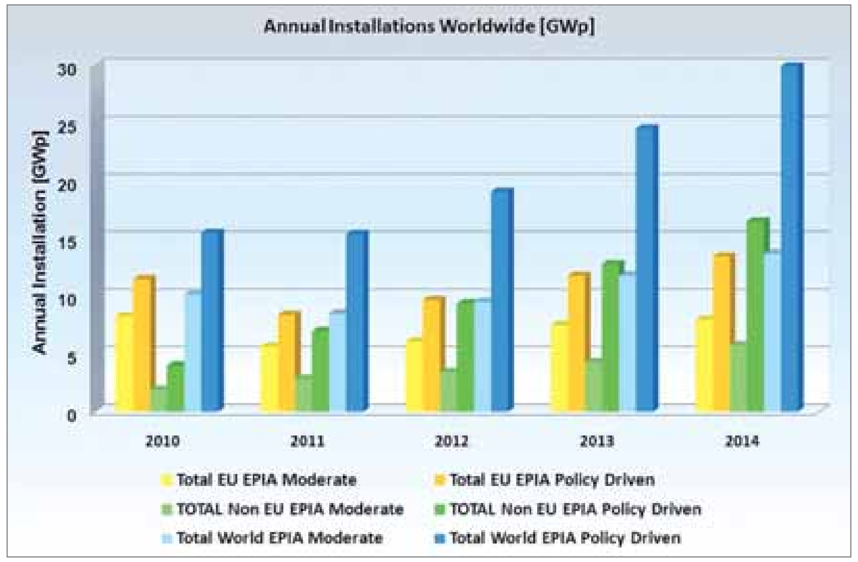
Designing for efficiency and reliability from renewable

By Peter Haaf

Solar electricity generation is becoming a viable alternative energy source, due to burgeoning energy costs. Up until 2007, the German solar market was the world's largest solar market driven by a law encouraging the use of renewable energy through incentives (the "Energieeinspeisungsgesetz").

Generating electricity from sunshine is taking the next step in market adoption, as the financial crisis seems to have been overcome. Panel prices have dropped further, and especially PV inverters have become a bottleneck for new installations. Earlier this year, the supply of PV inverters was so short that, for example, SMA in Kassel, the largest supplier of PV inverters with >38% market share worldwide, published an open letter to their customers on their website, apologizing for the shortage. As the markets in general seem to ease a bit, the same is not true for PV systems – other markets are taking the lead in terms of growth rates, in particular the USA and the emerging countries, as well as our European neighbours.

It is interesting to note that there is still a large gap between the "Policy Driven" market development, which would be in line with the targets for renewable energy shares of the various countries, and the "moderate" scenario, which is based on assumptions of manufacturing capacities and historic market development.



Expected market development
(Source: European Photovoltaic Industry Association, Update 2010)

Some other countries have taken the lead from Germany: in 2008 Spain had the largest amount of newly installed solar plant. Large growth in installed solar capacity is expected to come from Italy, France and the USA. The demand driven by these incentives has stimulated an increase in production capacity. The start of the recent world economic crisis and the sudden withdrawal of incentives from the Spanish solar market in 2008 have led to the supply of solar silicon exceeding demand at historic prices resulting in a price reduction of around 40%-50%. This brings photovoltaic technology closer to so-called "grid parity" where the cost of solar electricity equals the prevailing market price for electricity paid for by the consumer. Grid parity is now expected to occur sometime before 2015 for Germany.

Solar modules generate a DC voltage. A solar inverter converts this DC power into AC power which is then connected to the electricity grid. This article explores the new trends in solar inverter design. One important trend is to use higher power levels. Solar power farms with a peak capacity of over 100kW are becoming more popular. This trend is also seen for lower powered systems: the average power here is increasing from 5kWp to 10kWp.

For solar inverters, one very popular topology is the boost plus H-bridge topology, which is a two-stage, non-isolated topology. The first stage is a boost stage which increases the variable output voltage of the modules (e.g. in the range 100V – 500V) to a higher intermediate voltage, which must be more than the actual peak mains voltage (e.g. 230V x √2 OR >325V). This boost stage has second important function. To maximize efficiency, solar modules need to be operated to generate the maximum possible power. The power curve of a solar module is given by multiplying

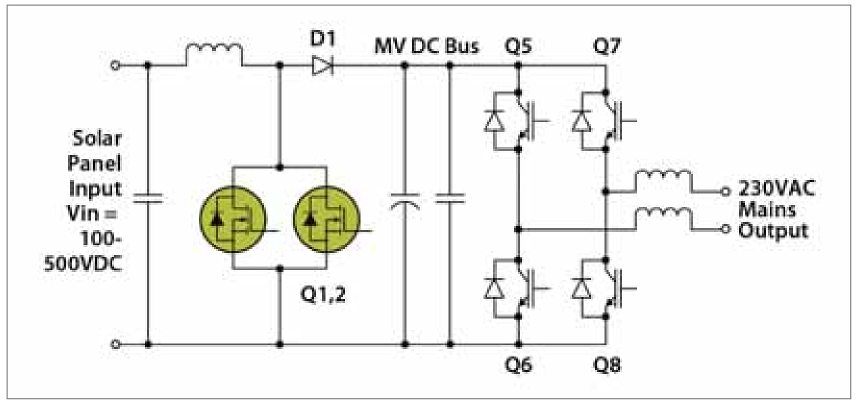


Figure 1: A popular solar inverter topology: boost + H-bridge

the output current and the output voltage characteristics. There is a maximum point in the power characteristics known as the "maximum power point" or MPP. This precise point varies with factors such as the type of module, temperature of the module and the shading of the module.

The input stage of the inverter tracks this maximum using a software technique called "maximum power point tracking" or MPPT, with the help of customized algorithms.

The second stage of the inverter converts the constant intermediate voltage into a 50Hz AC voltage which is fed into the mains supply. The output is synchronized with the mains supply phase and frequency. Since this stage is connected to the mains supply, it must achieve certain safety standards, even under fault conditions. In addition to this, there is a new draft proposal of the VDE 0126-1-1 linked to the Low Voltage Directive which requires that solar inverters should actively support the mains supply network in case of reduction in power quality which minimizes the risk of a more general power blackout.

Under current regulations, it is permissible to design an inverter that protects itself by simply switching off in the case of a power outage. However, if solar inverters become popular and provide a significant share of the generated power, simply switching off the connected solar inverters when there is a power outage could cause a larger mains

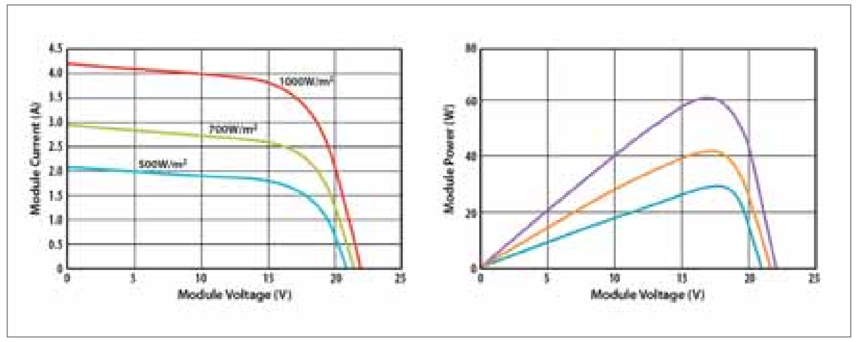
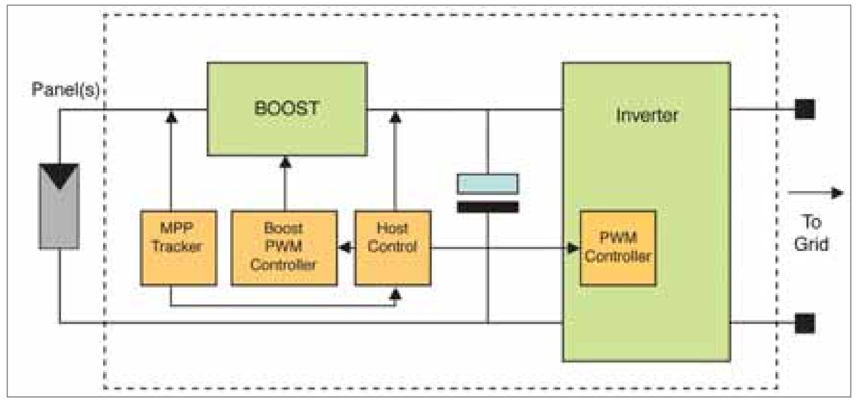


Figure 2: (Left) I-V characteristic of PV panel; (Right) P-V characteristic of PV panel



Block diagram of a PV inverter with the panels connected at the left side, and the grid on the right side

blackout, as one inverter after the other switches off and rapidly reduces the power available to the network. So the effect of the new draft directive will be to improve the stability and power quality of the mains distribution network at the cost of a slightly more complex inverter output stage.

Solar inverters need to be reliable, to minimize the cost of maintenance and downtime. These inverters need to be efficient, to maximize the amount of electricity generated and a considerable amount of effort is made by the designers of solar inverters to maximize the efficiency.

There are many ways to improve the efficiency of a boost converter. The boost converter can be operated in continuous or boundary conduction mode (CCM or BCM), leading to different optimization approaches. In CCM mode, one major source of losses is caused by the reverse recovery current of the boost diode. Here, silicon carbide diodes or Fairchild STEALTH™ diodes are generally used. BCM mode is more often used in solar inverters even if CCM mode is generally recommended for such power levels. The reason for this is that the forward voltage of the diodes used in BCM mode is a lot lower. BCM mode has a much higher ripple current in the EMI filter and the boost inductor. Good high frequency design of the inductor is one solution.

Looking closer at the current through the boost inductor, in continuous conduction mode the current never goes to zero but ripples around a relatively high input current, with the ripple being a smaller percentage of that input current. However, this means that the current in the diode will see an abrupt decrease when the main switch turns off, hence the need for a very fast rectifier with minimal recovery charge. When the converter is operated in boundary conduction mode, the current reaches zero in every switching cycle, and switching off the rectifier happens much softer. In combination with a silicon rectifier with very low recovery charge, like Fairchild's STEALTH™ diodes, highest efficiency is reached. Still, the current ripple is much larger now, and that can be improved with an interleaved converter, where two phases are operated out of phase, and their ripple currents will partly cancel. The resulting current ripple at the output is significantly lower. In conclusion, the combination of an interleaved boundary condition mode boost converter like Fairchild's FAN9612 and STEALTH™ diodes, highest performance can be achieved, as well as a very cost-effective solution.

A new approach is to interleave two boost stages instead of using one boost stage. This halves the currents flowing through each inductor and each switch. Further, the interleaving removes the input ripple current over a wide operating input range as the ripple current from one stage cancels out that of the other. Controllers such as the FAN9612 interleaved BCM PFC controller can handle solar boost stages without any problem.

There are two choices for boost switches in the inverter: IGBTs or MOSFETs. For input stages requiring switch voltage ratings of higher than 600V, fast switching 1200V IGBTs such as the FGL40N120AND are commonly used. For input stages where voltage ratings of 600V/650V are sufficient, MOSFETs are used.

Designers of the output H-bridge stage have historically used 600V/650V MOSFETs. New draft regulations have led to a renewed interest in using IGBTs in this area. These new regulations require four quadrant operation of the output stage.

In grid-connected applications like PV inverters, the grid quality is becoming more and more a concern, since these devices move power into the grid, by advancing the phase and / or the voltage, and that can lead to local overvoltages or increases in frequency. New regulations require the PV inverters to “control” the grid voltage, in an effort to keep both the voltage (230V +/-10%) as well as the frequency within tight limits (49Hz...51Hz), hence the need for the output stage of the PV inverter to be capable of operating in four quadrants, both delivering as well as absorbing energy. This requires the IGBTs in the inverter stage to be more robust and switching faster.

MOSFETs have built-in body diodes that have poor switching performance compared to the co-packaged diodes used in IGBTs. New field-stop IGBTs can switch voltages at a rate of 10V/ns which greatly improves the turn-on losses compared with older versions. The excellent soft recovery performance of the integrated diodes helps to reduce EMI caused by the high di/dt levels exceeding 500A/µs. For 16kHz-25kHz switching, IGBTs such as the FGH60N60UFD are recommended.

Another trend in the design of solar inverters is to increase the input voltage range, which results in a reduction in the input current at the same power level, or an increase in the power level with the same level of input current. Higher input voltages result in the need to use higher rated IGBTs in the range of 1200V, resulting in higher losses. One way of getting around this problem is to use a three-level inverter.

This trend is driven by efforts to increase the system efficiency, by

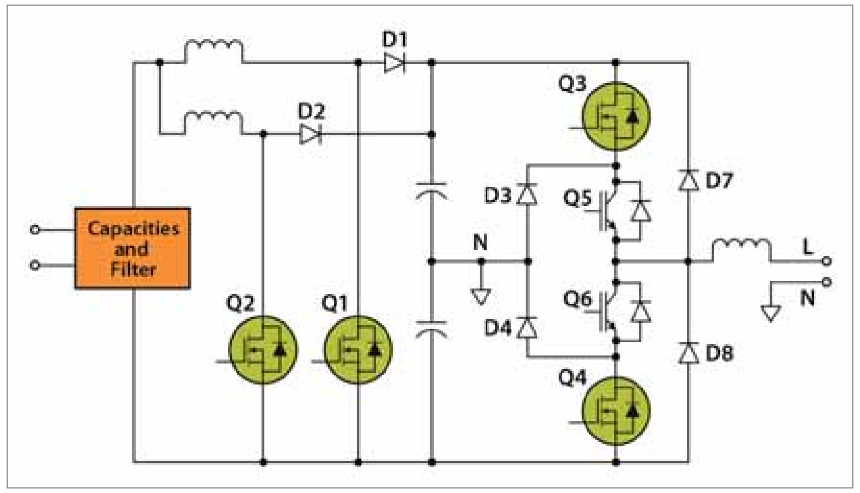


Figure 3: Solar Inverter Trend: interleaved BCM Boost + three level Inverter

connecting more panels in series, but also by new panel types, e.g. thin-film cells, that typically show a higher ratio of no-load voltage to voltage at the MPP. In inverter design, the target is to have maximum efficiency at the point where the string connected at the input has maximum power output, but the input structure must also be capable of surviving a higher input voltage in case of no power transfer to the grid, a no-load condition.

The high input voltage is divided into two by using two electrolytic capacitors in series. The midpoint is connected to the neutral line. 600V switches can now again be used. The three-level inverter can switch between the three levels: +Vbus, 0V and –Vbus. In addition to being more efficient than a solution built from 1200V switches, the three-level inverter has the additional advantage that the output inductors are much smaller.

For unity power factor, the function of the three-level inverter can be explained as follows: During the positive half-wave Q6 is always on, Q5 and Q4 are always off. Q3 and D3 form a buck converter which generated the output sine wave voltage. If only unity power factor is needed, Q5 and Q6 can be implemented as 50Hz switches using a very slow, very low Vce(sat) IGBT such as the FGH30N60LSD. If the power factor needs to be lower, Q5 and Q6 must operate at the switching frequency for a short time. The Diodes of Q3 and Q4 should be fast and soft recovery diodes. Q3 and Q4 could either be implemented as a fast recovery MOSFET such as the FGL100N50F or as fast IGBTs (FGH60N60SFD).

Based on these observations, it is likely that the three-level inverter topology will become popular for non-isolated inverters with power levels above 5kWp because of the possibility of achieving efficiencies of over 98%.

Author: By Peter Haaf,
Technical Marketing Manager
Fairchild Semiconductor GmbH
Fuerstenfeldbruck, Germany

www.fairchildsemi.com

LI-ION BATTERY CIRCUIT PROTECTION

New technology focuses on emerging applications

By Ty Bowman

Technological advances in lithium ion (Li-ion) batteries have enabled high-power Li-ion cells with higher energy density and lighter weight to replace Nickel-Cadmium (NiCd) batteries – and even lead acid batteries – in applications such as power tools, e-bikes, light electric vehicles (LEVs) and back-up power supplies.

Li-ion technology is more environmentally friendly than the NiCd or lead acid technologies; however, the challenge for the adoption of Li-ion batteries by these new markets is the greater emphasis by system designers on battery safety requirements compared with NiCd or lead acid technologies.

A new approach to Li-ion battery pack circuit protection confronts these market challenges by offering an alternative to conventional higher-cost, space-consuming protection technologies. This new hybrid technology connects a bimetal protector in parallel with a PPTC (polymeric positive temperature coefficient) device. The resulting Metal Hybrid PPTC (MHP) device helps provide resettable overcurrent protection in high-rate-discharge battery packs while also utilizing the low resistance of the PPTC device to help prevent arcing in the bimetal protector at higher currents and by heating the bimetal to keep it open and in a latched position.

The initial device introduced, the MHP30-36 device, has a 36VDC/

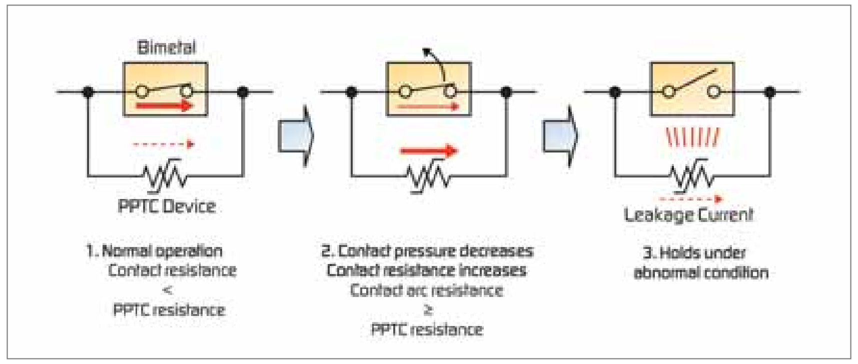


Figure 1. Activation steps of the MHP device

100A maximum rating and a hold current of 30A. However, MHP device technology can be configured for various applications and higher voltage (up to 400VDC) and hold current (60A) devices are currently in development.

The conventional approach
Many of the conventional circuit protection techniques for high-rate-discharge Li-ion applications tend to be large, complex or expensive. Some circuit protection design approaches might use a combination of ICs and MOSFETs or similar complex solutions. Other designs might consider a conventional bimetal protector in DC power applications requiring 30A+ hold current, but the contacts must be large enough to handle the high current, resulting in an overall device size that is much larger. Additionally, the number of switching cycles must be limited due to contact damage that may result from arcing between the contacts.

In comparison the new MHP hybrid device can replace or help reduce the number of discharge FETs and accompanying heat sinks used in some complex IC/FET battery protection designs. The MHP device offers space-reduction, cost-reduction and protection-enhancement benefits for high-rate-discharge Li-ion battery pack applications.

How it works
During normal operation, current passes through the bimetal contact due to its low contact resistance. When an abnormal event occurs, such as a power tool rotor lock, higher current is generated in the circuit causing the bimetal contact to open and its contact resistance to increase. At this point, the current shunts to the lower resistance PPTC device and helps prevent arcing between the contacts while also heating the bimetal, keeping it open and in a latched position.

As shown in Figure 1, the activation steps of the MHP device include:

1. During normal operation, because contact resistance is very low, most of the current goes through the bimetal.
2. When the contact begins to open, contact resistance increases quickly. If the contact resistance is higher than the PPTC device's resistance most of current goes to the PPTC device and no — or less — current remains on the contact, therefore preventing arcing between the contacts. When current shunts to the PPTC device, its resistance rapidly increases to a level much higher than the contact resistance and the PPTC heats up.
3. After the contact opens, the PPTC device starts to heat up the bimetal and keeps it open until the overcurrent event ends or the power is turned off.

A PPTC device's resistance is much lower than that of a ceramic PTC. This means that even when the contact opens just a small amount the contact resistance increases only slightly and the current can be shunted to the PPTC device and help prevent arcing on the contacts. Typically, the resistance difference at room temperature between ceramic and polymer PTC devices is in the range of two decades (x10^2); so when the higher resistance ceramic PTC devices are combined in parallel with a bimetal they are less effective than the MHP device at suppressing arcs at higher currents.

Figure 2 shows a circuit diagram of the bimetal protector and PPTC device in parallel.

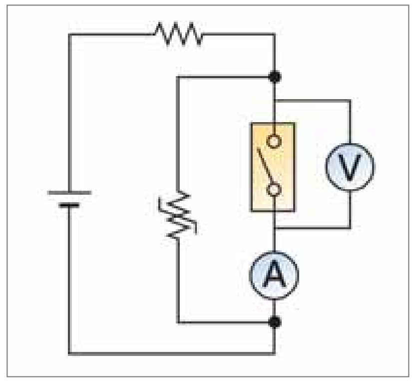


Figure 2: PPTC device/bimetal protector parallel circuit

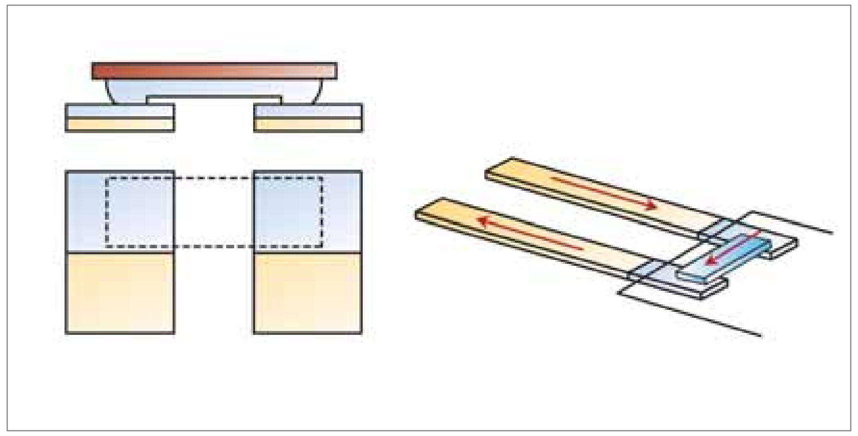


Figure 3: Double-make/double-break contact design used for the hybrid MHP device

Smaller contact size and lower resistance
On a typical bimetal protector the contact is located in only one place so it may exhibit weak voltage-withstand characteristics. Because higher currents would require a much larger form factor in a single contact design, the MHP device uses a type of contact that is referred to as "double-make" or "double-break" design in order to downsize the device (Figure 3).

This technology offers several advantages as compared to a typical bimetal protector:

1. The device exhibits very low resistance because the current path is very short;
2. heat is only generated at the contact point, permitting the use of thermal control to achieve precise thermal activation; and
3. It enables MHP devices to have a smaller form factor compared to other breaker devices with a similar rating.

In comparison, with a standard bimetal contacts, the contact is located in only one place so it generally has weaker voltage withstand characteristics than the MHP device.

Impact/Shock withstand improvement
A specific advantage of the MHP device is that it can be used in the harsh operating environments of high-current applications by providing longer cycle life and high vibration/shock withstand.

A typical power tool battery pack operates under severe vibration and impact conditions. To meet these requirements, the MHP device needs sufficient contact pressure between the contacts. Standard protector devices typically use an arm with strong spring tension to keep the movable contact on the fixed contact. But the spring tension is usually insufficient to maintain contact pressure under strong impact or vibration conditions — even if a strong spring is used.

To overcome this challenge, design efforts for the MHP device focused on the bimetal disc, since a formed bimetal disc has sufficient strength to stay flat when there is no heat or thermal contact. In addition, a "hook" was added to the movable arm to enhance the contact pressure provided by the bimetal disc. The movable arm is a cantilever held by a pin located on the other side of the device. When a hook is added close to the contact, the movable arm rotation is reduced, resulting in a robust downward force on the two contacts. The initial MHP device for power tool battery applications is rated to survive at least 500 cycles and survive a 1500g drop test without failure, and as many as three cycles at 3000g.

The first device available in a planned family of MHP devices, the MHP30-36-T device, has a 36VDC /100A maximum rating and a time-to-trip of less than five seconds at 100A (@25°C). The device's hold current is 30A and the initial resistance is under 2mohms, which is less than typical bimetal protectors that are generally rated at 3 to 4mohms.

Figure 4 shows the shape and dimensions of the new MHP30-36 device, which is rated at 30A hold current and is the same size as a typical bimetal protector with only a 15A rating. Additionally, the device has flat corners on one side so that it fits snuggly between standard 18mm diameter Li-ion cells in a battery pack.

Summary
The rapidly expanding market for high-rate-discharge Li-ion batteries is generating new requirements for battery circuit protection devices

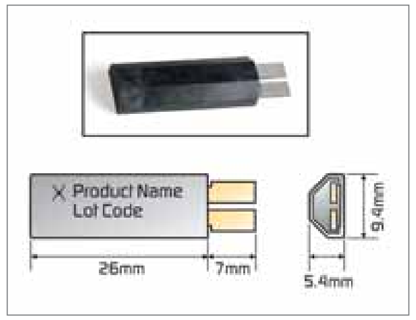


Figure 4. MHP30-36 device dimensions

that are capable of handling these higher current and voltage ratings. The new MHP hybrid device offers battery pack designers a new circuit protection approach that makes these designs more cost-effective. Compared to conventional approaches, this hybrid device offers enhanced protection against arcing while eliminating the need for the larger and multiple discharge FETs and accompanying heat sinks required in previous IC-plus-FET battery protection designs.

By using PPTCs in parallel and selecting PPTCs with different voltage ratings, MHP designs can be configured for a broad range of applications. The MHP device' s construction can be configured for various applications, and higher voltage (up to 400VDC) and hold current (60A) devices are currently in development.

Additional design concepts are under development incorporating a third terminal as a signal line so the MHP device can take advantage of the advanced features of the IC to monitor the battery's various vital functions. If an abnormality is detected, the IC can send a signal via a low power switch line to activate the device and open main line. This line of MHP devices with "smart activation" will provide more control over circuit protection in large Li-ion battery packs and modules such as those used in solar power systems and other back-up power applications.

Author: Ty Bowman
Global Battery Market Manager
Circuit Protection Business Unit
Tyco Electronics

www.circuitprotection.com

NTC CHIPS FROM WAFER TECHNOLOGY

The logical choice for embedded applications

By David Connett

The accuracy of the wafer coupled with assembly processes already commonly found in the manufacturing plants of IGBT modules, makes the chip form of NTC the ideal component for embedding into power electronic modules.

The need for thermal management in today's semiconductor devices, such as IGBTs or LEDs, is well documented in the internet. Not so much is how this should be achieved.

Thermistor based Sensors.
Thermistors (temperature dependent resistors) are ideal components for the measurement of temperature. Available with Positive Temperature Coefficients (PTCs) with a resistance that increases with rising temperature and Negative Temperature Coefficient (NTCs) that feature a declining resistance with increasing temperature, thermistors can be found in many electronic systems for temperature sensing and over-temperature protection.

Conventional NTCs are either in EIA SMD sizes (0402, 0603, 0805 etc) or leaded and are designed for PCB mounting. Some probes are available for mounting on heat-sinks but these, due to their application, tend to be large robust and hermetically sealed packages which limit their deployment in the majority of embedded semiconductor not only due to their size but also to the problems of termination.

However, due to their compact nature SMD technology is widely used for embedded applications within semi-conductor modules despite that fact that there are a number of difficulties that must be overcome in the module assembly process. These problems can be summarised as follows:

1. The terminations must be located on the substrate in the form of pads (either for soldering or for gluing)
2. The part is generally delivered on tape or in a cassette
3. The surface of the actual NTC is not always in contact with the substrate to which it is attached
4. The differing temperature coefficients between the NTC material and the substrate can lead to cracks

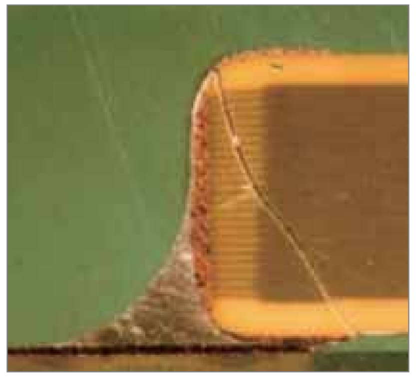


Figure 1: Crack in Ceramic (for clarity a MLCC is shown)

5. The over-moulding process can also place additional mechanical stresses on the body but also the terminations which can also lead to cracks in the ceramic

Whereas the majority of these issues can be overcome with the necessary investment in processes and machinery, the problem with cracking, (Fig.1) which is mostly due to the soldering and assembly process, is not so easily solved. Even if the process can be optimised during the assembly

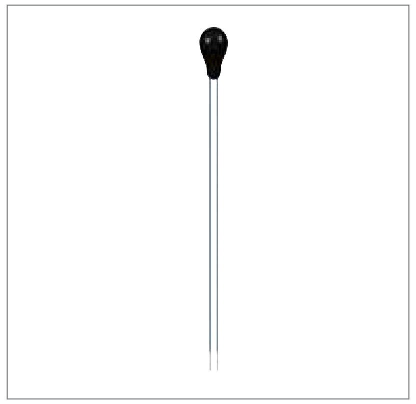


Figure 2: Minisensor

Figure 3: NTC Chip in Wafer Technology

process (control of the placement pressure, centralising of pick and place head etc), the problem of the potential forming of cracks due to the temperature cycling of the NTC through the semiconductor itself during the lifetime of the product itself will always remain unsolved and overtime can therefore still become a quality issue.

The solution here is to use an assembly process that is already widely used within the semi-conductor manufacturing industry

Figure 4: Finished Chip

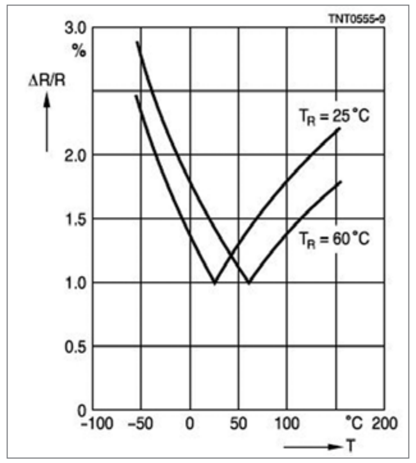


Figure 5: Temperature tolerance for TR = 25 °C and 60 °C

itself:

NTC Chips

TDK-EPC has used a wafer based technology for many years in its manufacturing process of so-called mini-sensors (Fig.2). The advantage of this technology versus the deployment of a SMD device or disc is that the dicing process is physically linked to the electrical properties of the complete wafer (Fig.3). Hence the dicing process, in combination with appropriate trimming for the finished chip, can be realised with extremely tight tolerances.

An additional advantage of the wafer technology for chip NTCs solves the problem of the electrical connection. As the terminations are no longer on the component edges (as with a SMD) but on the top and bottom surfaces (Fig. 4) direct contacting to the module substrate on one side and wire bonding for the second connection are now possible. Hence the solder process can also be eliminated.

Rated Temperature

However, the major advantage that is especially beneficial for the

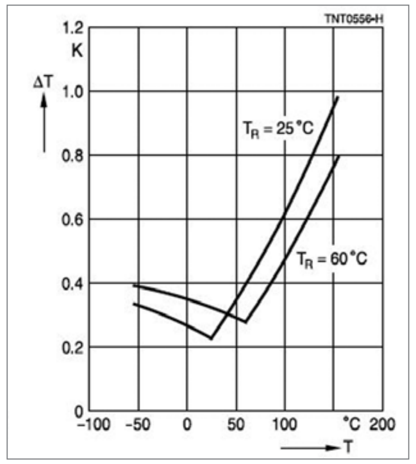


Figure 6: Resistance tolerance TR = 25 °C and 60 °C

semi-conductor industry, is that the temperature for this measurement process and hence the subsequent dicing can be undertaken at higher temperatures – typically 100°C.

Through this, the inaccuracies of the NTC R/T characteristics can be for the most part eliminated and as a result the IGBT can be safely operated much closer to its' maximum junction temperature limits.

The reason for this better measurement control can be explained as follows:
The difference in tolerance between a rated resistance at 25°C and 60°C can be expressed in D resistance (Fig.5) and in D temperature (Fig.6). The maximum accuracy is hereby achieved at the rated temperature.

However in addition to the resistance tolerance, the accuracy of the B-Value should not be ignored since also defines the precision of the temperature measurement. By definition a lower B-Value tolerance results in a more accurate result (Figs.7 and 8).

The net result of these critical

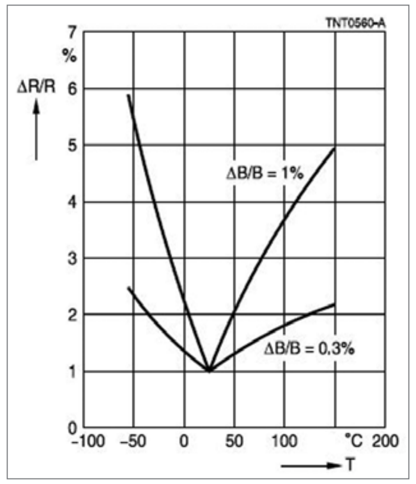


Figure 7: Resistance tolerance DB/B = 0.3% and 1.0%

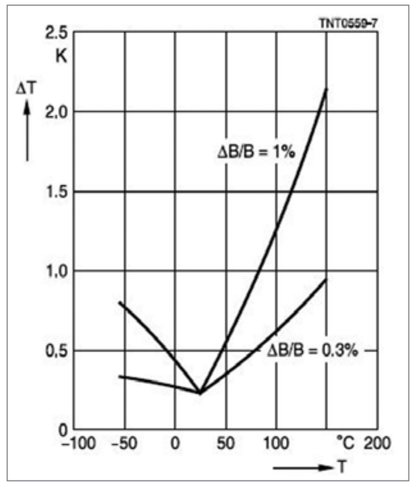


Figure 8: Temperature tolerance DB/B = 0.3% and 1.0%

parameters can be seen in the change of resistance over temperature between a Chip rated at 100°C and a SMD rated at 25°C (Fig. 9). With a change in resistance of up to ± 5°C at 115°C for the 0603 SMD (3% B tolerance; 5% R25 tolerance) the microcontroller will need to reduce the power of the IGBTs at 120°C to ensure that the junction temperature does not exceed 125°C whereas due to the inaccuracy of the NTC the actual junction temperature may only be 115 °C.

The wafer rated at 100°C (1% tolerance, 3,5% R100 tolerance) would have a temperature inaccuracy of only ± 1.5°C at 120°C meaning that power derating is only necessary at 123°C to ensure a safe junction temperature assuming 125°C is its' limit.

It should also be pointed out that with the SMD these conditions only apply to the delivered state, an additional drift of up to 3% needs to be considered after the soldering process.

An additional advantage of this technology is that the maximum operating temperature is 155°C and this depending on IGBT requirement could be increased to 175°C and the B-Value tolerance could be further tightened to 0.5%.

Terminations

The terminations of the chip surface can be adapted to the mating surfaces with a silver electrode or gold if this is more desirable for the wire bonding process.

Certification

Recognition by Underwriters Laboratories according to UL 1434 has already been secured.

Summary

Hence the accuracy of the wafer coupled with assembly processes already commonly found in the manufacturing plants of IGBT modules, makes the chip form of NTC the ideal component for embedding into power electronic modules.

For more information on these devices and their application please contact:
design-solutions@epcos.com

Author: By David Connett
Director IC Reference Design
EPCOS AG
Germany

www.epcos.com

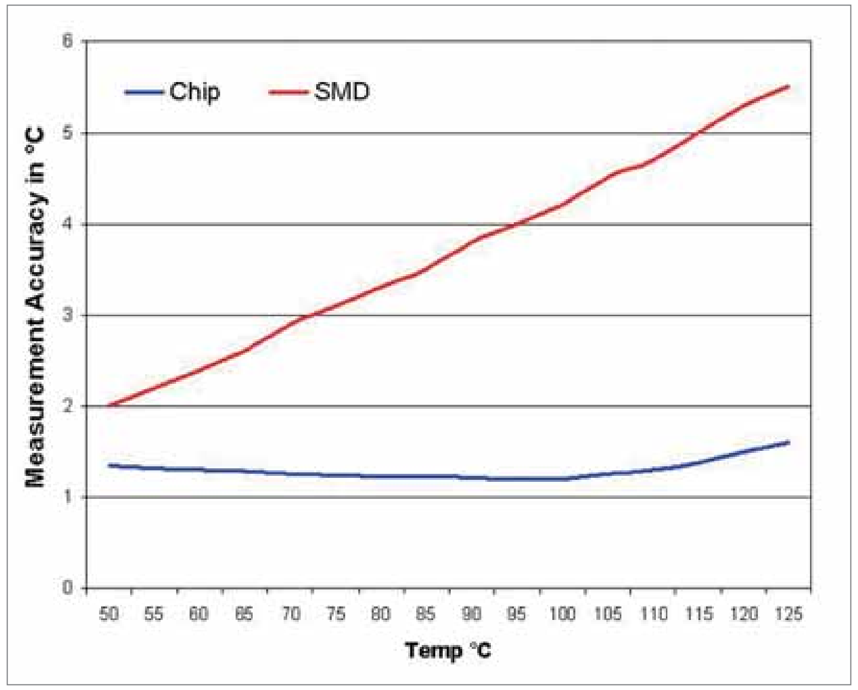


Figure 9: DTemp in °C between Chip rated at 100°C and a SMD rated at 25°C

Special Report: Renewable Energy

PSD EUROPE
Power Systems Design: Empowering Global Innovation

Inside:

RENEWABLE ENERGY & ENERGY SAVING

Environmental opportunities for the power electronics industry

By Alberto Guerra

The global economic recession of the last two years has had a profound impact on world energy demand, at least in the near term. As manufacturing and consumer demand for goods and services declined so did energy consumption with a cumulative 3.4% decline from year 2008 to 2009.

World energy consumption is forecast to increase 49% by 2035, with growth in demand in emerging countries projected to grow by a staggering 89% in the industrial, transportation and residential segments driven by the vast new middle-class of consumers.

At the same time, the contribution of renewable energy use for electricity generation will grow steadily to reach 23% of the total by 2035 with much of the increase by hydropower wind power and solar power. Of the 4.5 trillion kilowatt-hours of increased renewable generation by 2035, 54% will come from hydroelectric power, 26% from wind, while 15% from Solar PV and Thermal.

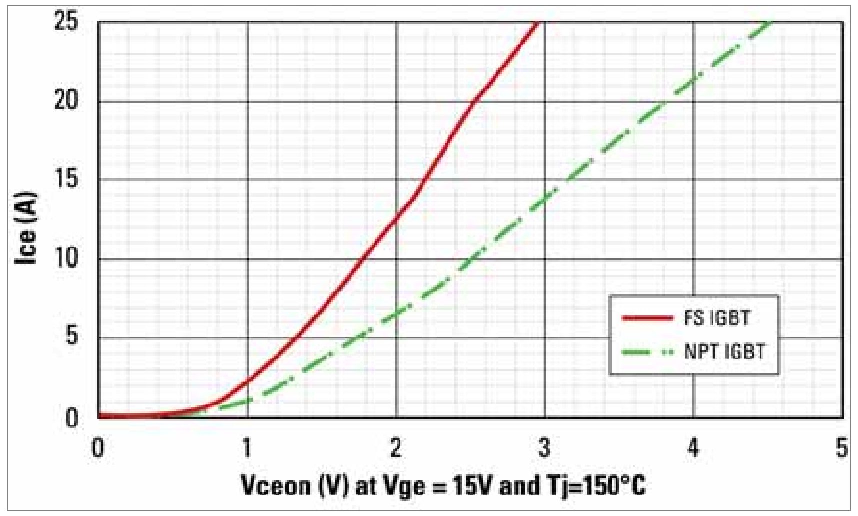


Figure 1: VCE(on) comparison of FS (Red), and NPT (Green) IGBTs

As the demand for greener appliances and consumer products soars across the globe, and energy savings becomes a global necessity, solar and wind power technologies begin to proliferate in cities and states around the world. Concurrently, smart grid and smart meter deployments are also on the rise. This renewable energy growth is further fueled by the recent economic stimulus package passed by the present administration, which calls for spending $45 billion on alternative energy including some $4.3 billion on smart electric grids.

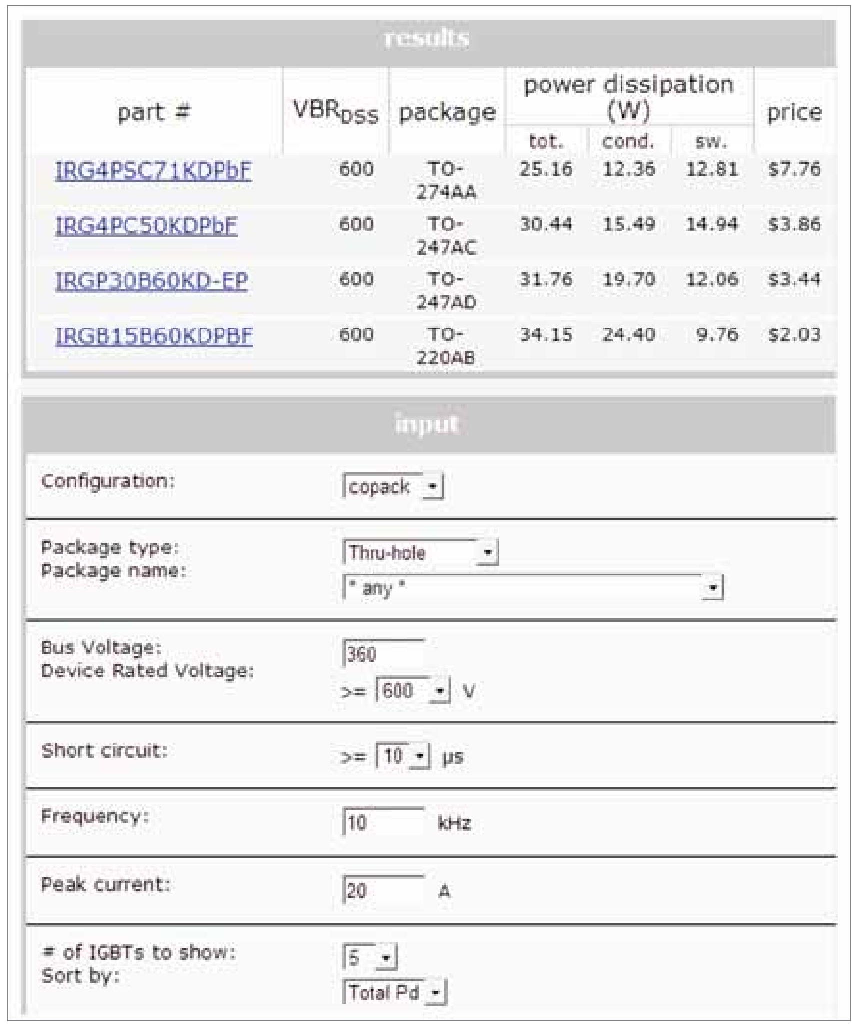
At the same time private sector groups like the Association of Home Appliance Manufacturers (which includes in its ranks the top manufacturing companies in the appliance sector) are now the promoters of advanced energy savings initiatives to study how, by implementing changes in the home appliance efficiency standards and increasing product energy efficiency, save more than 9 quads of energy over 30 years (The US uses ~100 quads), up to 5 trillion less gallons of water and reducing GHG emissions by ~550 MMT CO2 over a 30-year period.

Now, in this transformation, energy efficient power converters and power management devices are playing an ever increasing critical role by de facto enabling the successful deployment of any meaningful energy saving initiative in the residential and industrial sectors, so the power management manufacturers have a fundamental business and ethical motivation to stay ahead in technology development and innovation.

Saving energy

Since its inception some 60 plus years ago, International Rectifier's mission has been to minimize power losses and to save power via efficient power conversion solutions. With that goal in mind, IR has pioneered many innovations over the last six decades, including commercial introduction of Solar cells in the late fifties. These cells were used to power the initial fleet of American satellites enabling for the first time weather monitoring and real time television global broadcasting.

Today, IR offers a large portfolio of high performance power management products for the Renewable Energy (Solar & Wind) industry. From string inverters for residential, commercial and utility level applications to micro-inverters and DC-DC converters, IR has generated leading edge power semiconductor devices that are positively changing the photovoltaic (PV) inverter landscape. For instance, IR's state-of-the-art MOSFETs and insulated gate bipolar transistors (IGBTs) are dramatically lowering power losses while improving efficiencies in PV inverters.



results

part #	VBR_{DSS}	package	power dissipation (W) tot.	cond.	sw.	price
IRG4PSC71KDPbF	600	TO-274AA	25.16	12.36	12.81	$7.76
IRG4PC50KDPbF	600	TO-247AC	30.44	15.49	14.94	$3.86
IRGP30B60KD-EP	600	TO-247AD	31.76	19.70	12.06	$3.44
IRGB15B60KDPBF	600	TO-220AB	34.15	24.40	9.76	$2.03

input

Figure 2: Screen shot of IR's IGBT selection tool

In the IGBT sector, for instance, IR offers a broad portfolio with voltage ranges spanning from 600V to 1200V, supporting the power needs of high performance inverters from 5kW to 30kW and above. While a number of process technologies have been developed to manufacture IGBTs, and each can be selectively optimized for specific PV inverter topology, the rapid adoption of field-stop (FS) trench technology is gaining momentum.

Unlike the standard IGBT wafers which are 300µm thick, the FS IGBTs are thinned down to a minimum thickness of 70µm. As a result, it improves switching performance, and reduces the conduction path to improve collector-to-emitter voltage (VCE(on)) characteristics (Figure 1).

IR's thin IGBT technology is housed in TO-220/D2PAK and TO-247 industry standard packages for use in applications up to 5kW in order to lower system costs.

In order to support power electronic engineers to design more efficient converters, and at the same time reducing the time to market of the product, IR has a new online IGBT selection tool that enables design optimization in a wide

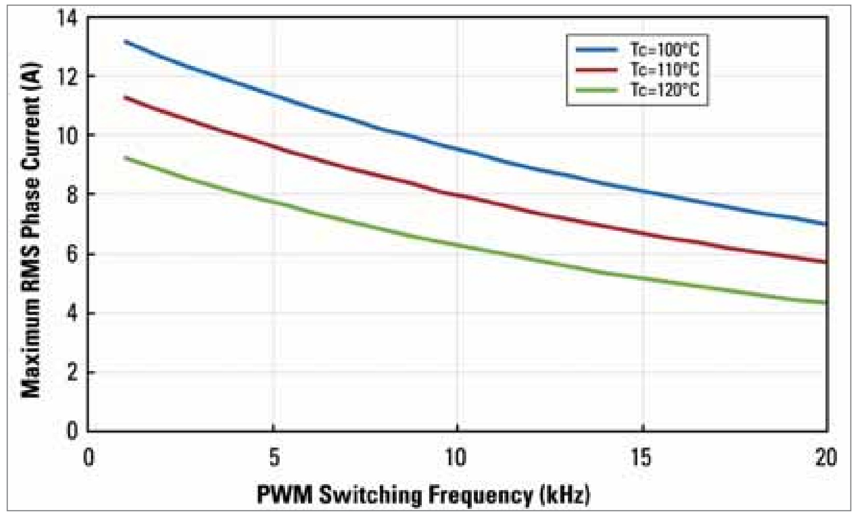


Figure 3: Current vs. Switching Frequency chart for an IRAM module over a range of temperatures

range of applications including motor drive, uninterruptable power supplies (UPS), solar inverters, and welding. The new selection tool helps designers make use of IR's broad IGBT portfolio and weigh the performance tradeoffs (Figure 2).

IGBT selection requires evaluation of many parameters that cannot be simplified into a single metric so the new online selection tool enables engineers to quickly and easily compare choices to select the optimal IGBT for their design.

For higher power PV inverters (such as 3-phase grid with power output >10kW) IR IGBT chips are used in power modules, a more rational and efficient solution than discrete components at this power level. Incidentally, power modules using IGBTs have already been field proven in terms of reliability and performance in applications like variable frequency motor drives, high power UPS and welding machines where IR chips are adopted and used by many module manufacturers.

That enables the growing PV inverter industry to quickly capitalize on the infrastructure and quality and reliability standards already in place for these products.

Another product in IR's portfolio specifically developed to enable implementation of cost effective solution in energy savings products (i.e.; air-conditioning units, washing machines, etc.) is the IRAM intelligent power module. Capable of incorporating high voltage drivers, IRAM offers higher integration for a variety of power inverter/converter topologies. This lowers external component count, and simplifies assembly processes to lower system cost and achieve faster time to market. Additionally, fewer components and simpler assembly translates into better overall product reliability.

In order to help designers in selecting and designing with these products, IR has made available a specific web-based tool that can greatly simplify the calculations necessary to correctly choose a power stage for example in motor drive applications by precisely estimating current ratings and total power dissipation (Figures 3-5). These ratings are much more useful than typical DC ratings that are normally found in product datasheet because they show the capability of the power module in real application conditions.

Optimized Power Devices

Meanwhile, for emerging power electronics such as PV micro-inverters and micro-converters (DC-DC) optimized for single PV panels, IR has developed a family of advanced trench MOSFETs in the medium voltage range (40V to 150V) with benchmark performance

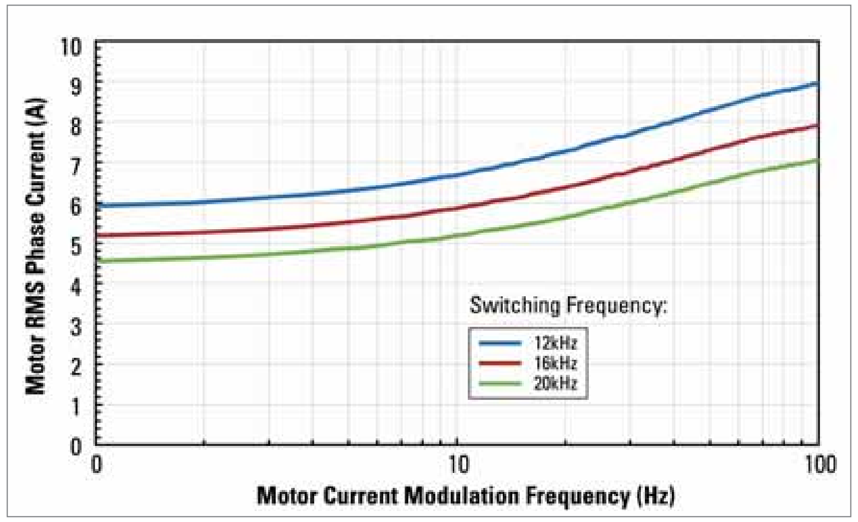


Figure 4: Current vs. Modulation Frequency chart for an IRAM module over a range of switching frequencies

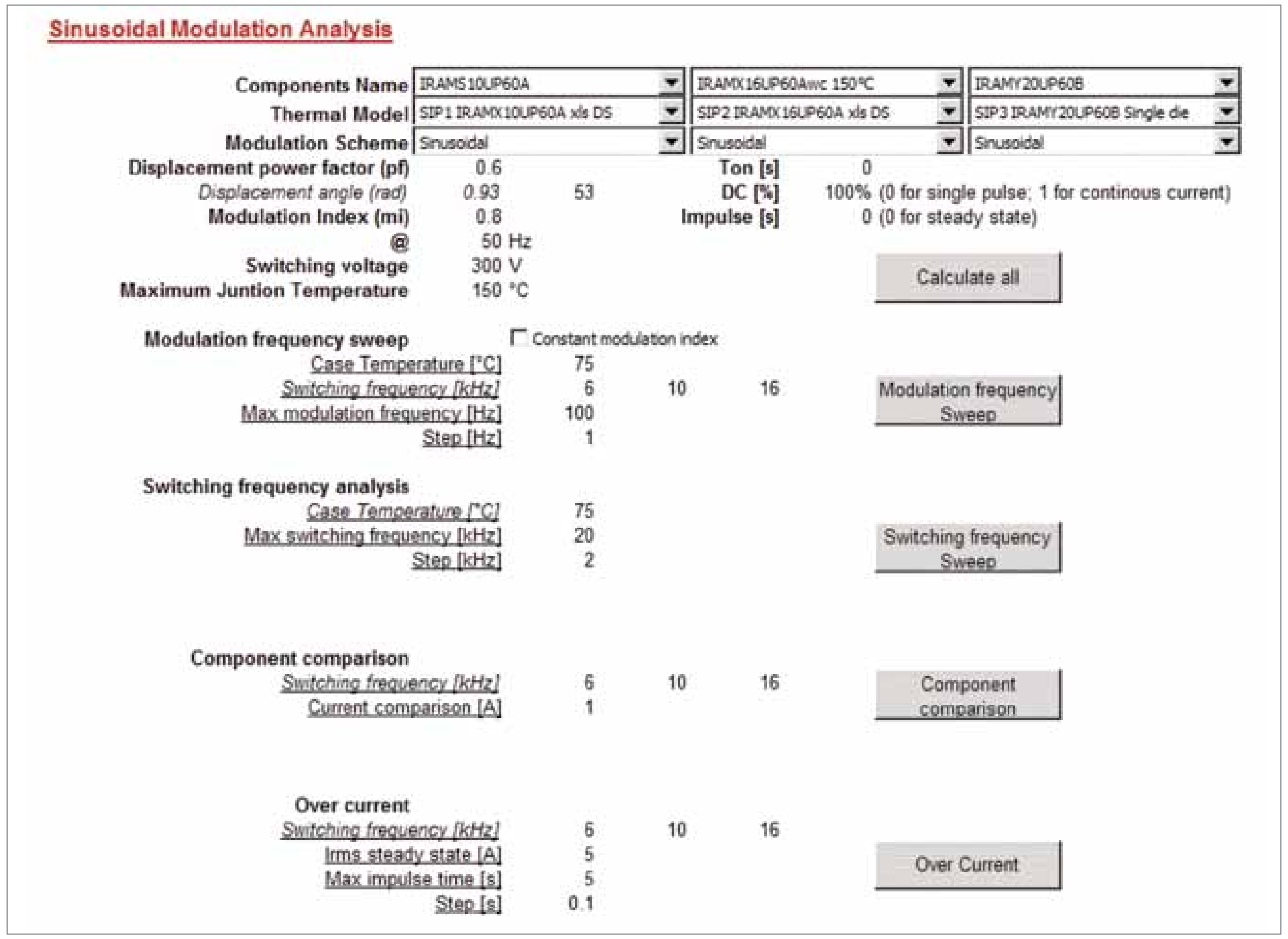


Figure 5: Screen shot of IR's IRAM simulation tool

in conduction losses. Thermally optimized, these MOSFETs are tailored for DirectFET®, an innovative packaging technology pioneered by IR.

Interestingly, the emphasis on the reliability of components is a characteristic of the solar industry, where the life expectancy is very high. In fact, 20-25 years is the norm for the regular warranty. Although, this level of reliability is not intrinsically a problem for mature power semiconductor devices, it could certainly raise concerns for passive components, especially capacitors. By adopting circuit topologies, such as soft switching versus hard switching, that reduce stress over these components, designers can address the reliability requirements of solar applications. That requires using the right combination of IGBT characteristics, such as breakdown voltage, VCE(on), turn-off time, switching speed, and conduction loss.

The wide array of IGBTs and power MOSFETs available in IR's portfolio gives designers ample choice to address this challenge.

There is global demand for clean, low cost sources of energy and a challenge to meet the projected level, specifically in the emerging countries (that by the time will be clearly fully "emerged"). The recent Gulf of Mexico's massive oil spill, and other devastating environmental disasters caused by similar accidents, is a grim reminder of the threat to our environment.

Renewable energy is the answer. Energy policies of industrialized and emerging countries have become more favorable toward renewable energy, further driving its growth and adoption worldwide.

Although, the direct impact on wind and solar industry will be partially modulated by different levels of subsidies and tariffs, growth is unstoppable. And with that the demand for power semiconductor devices used in all renewable energy segments will surge.

Author: Alberto Guerra
International Rectifier
El Segundo, California, US

www.irf.com

THE ENERGY HARVEST

Harvesting power from previously unusable low-current sources

By Steve Knoth

Shunt voltage references are simple to use; they have been around for many years and are in a myriad of products. However, they cannot effectively charge a battery, and to configure one to do such a task can be extremely cumbersome.

To-date, the ability to accurately and safely charge a Lithium-Ion/Polymer, coin cell or a thin film battery from a low-current source or an intermittent harvested energy type source has been unachievable.

Embryonic in the market place, energy harvesting ICs can convert a transducer's signal into an input appropriate for a battery charger device. Recent technology developments have pushed energy harvesting to the point of commercial viability, even though it has been emerging since early 2000. In 2010, a "growth" phase is imminent for this technology.

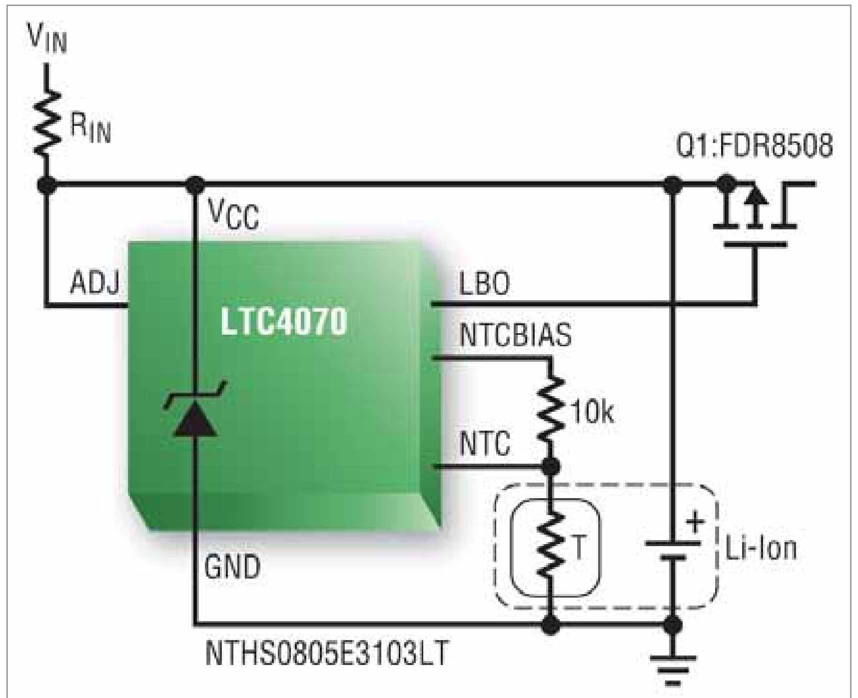


Figure 1: LTC4070 application circuit operational modes

The opportunities in energy harvesting applications are widespread:

- Replace or recharge battery powered systems in situations where battery replacement is inconvenient, impractical or dangerous
- Eliminate the need for wires to carry power or to transmit data
- Smart wireless sensor networks to monitor and optimize complex Industrial processes, remote field installations and building HVAC
- Harvesting otherwise wasted heat from industrial processes, solar panels, internal combustion engines
- Various consumer electronic accessory chargers

Many of these applications inherently have intermittent or low-power sources. On the battery side, although technology has improved, portable electronic device batteries still require protection and conditioning to keep them running optimally. Lithium-Ion/Polymer batteries are a mature technology and a popular choice to power many electronic devices due to their high energy density, low self-discharge, low maintenance, and wide voltage range, among other features. Coin cells offer high energy density, stable discharge characteristics and low weight in a small form factor. Thin film batteries are an emerging technology with such benefits as a high number of charge cycles and physical flexibility, i.e. they may be formed to fit in almost any shape depending on the end application. However, some potential detrimental effects on these batteries exist if not properly charged and conditioned.

Design challenges for low power consumption chargers

An adjustable shunt reference can be programmed for an appropriate battery float voltage, but it will lack the NTC function of a battery charger. More importantly, the required operating current is so high that battery charging from low power or intermittent sources is not practical. Alternatively, a discrete shunt reference can be built from a Zener diode, resistors, an NPN transistor, and comparators for the NTC function. However, it will still suffer from the same limitations outlined above. Additionally, it will be cumbersome to implement and will consume much valuable PCB area by comparison.

Typical battery charger ICs require a constant DC input voltage and cannot handle bursts of energy. However, intermittent energy harvesting sources such as indoor photovoltaic arrays or piezoelectric transducers provide bursts of power. A unique IC with sub-1uA quiescent / operating current is necessary to charge a battery from this type of energy source. Lithium-Ion/Polymer chemistry batteries provide the high performance features necessary for portable electronic devices but must be treated with care. For example, Lithium-Ion/Polymer cells can become unstable if charged over 100mV beyond their recommended float voltage. Further, simultaneous instances of high voltage and high temperatures adversely affect battery life, and in extreme cases can lead to their self-destruction. In addition to potential adverse effects of simultaneous high temperature & high voltage, coin cells and thin film batteries have capacity issues due to their small form factor.

Shunt architecture basics & benefits

A shunt reference is a current-fed, two terminal device that draws no current until the target voltage is reached. A shunt reference is used like a Zener diode and is often shown on a circuit schematic as a Zener diode. However, most shunt references are actually based on a bandgap reference voltage.

A shunt reference requires only a single external resistor to regulate its output voltage making it extremely easy to use. There is no maximum input voltage limit, and the minimum input voltage is set by the value of the reference voltage because some headroom is required for proper operation.

Further, shunt references have good stability over a wide range of currents. Many shunts are also stable with large or small capacitive loads.

A simple solution

Any solution to satisfy the battery charger IC design constraints outlined above would have to combine a shunt regulator's characteristics and those of a battery charging IC with the ability to charge from low power continuous or intermittent sources. Such a device would also need to protect and extract the maximum performance from a Lithium-ion/Polymer battery, coin cell, or thin film battery.

Linear Technology has developed the industry's first shunt-architecture battery charger. The LTC4070 is an easy-to-use, tiny shunt battery charger system IC for Li-Ion/Polymer batteries, coin cells, or thin film batteries. With its 450nA operating current, the IC protects batteries and charges them from previously unusable very low current, intermittent or continuous charging sources. The LTC4070's charge current may be boosted from 50mA up to 500mA with the addition of an external PMOS shunt device. An internal thermal battery conditioner reduces the float voltage to protect Li-Ion/Polymer cells at elevated battery temperatures. Multiple-cell battery stacks can be charged and balanced by configuring several LTC4070s in series. Housed in a low profile (0.75mm) 8-lead 2mm x 3mm DFN package, the LTC4070 provides a complete and ultra-compact charger solution with just a single external resistor required in series with the input voltage. The device's feature set suits it well for both continuous and intermittent, lower power charging source applications including Lithium-Ion/Polymer battery backup, thin film batteries, coin cell batteries, memory backup, solar-powered systems, embedded automotive and energy harvesting.

With pin-selectable settings of 4.0V, 4.1V, and 4.2V, the LTC4070'

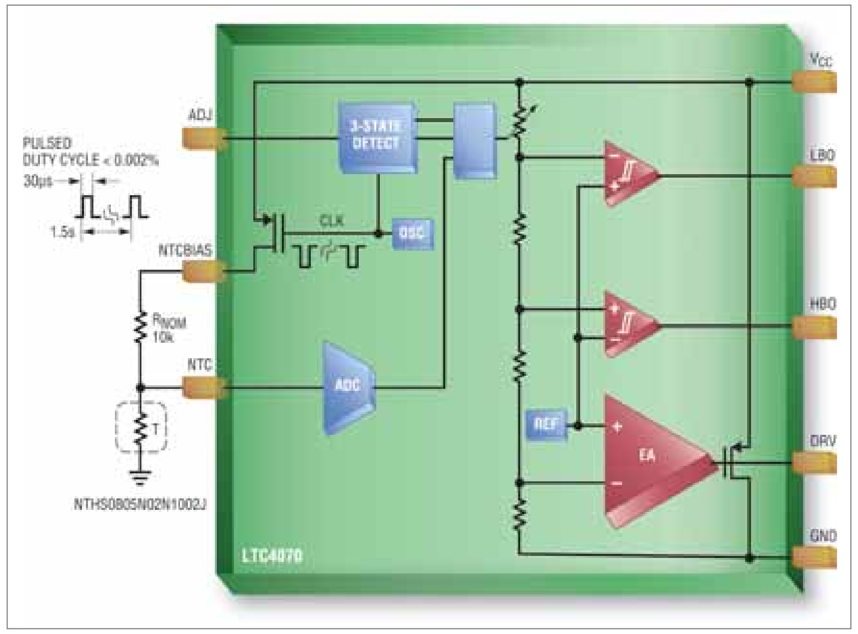


Figure 2: LTC4070 block diagram

s 1% accurate battery float voltage allows the user to make tradeoffs between battery energy density and lifetime. Independent low battery and high battery supervisory status outputs indicate a discharged or fully charged battery. In conjunction with an external PFET in series with the load, the low battery status output enables a latch-off function that automatically disconnects the system load from the battery to protect the battery from deep discharge.

In addition to its compact 2mmx3mm 8-lead DFN package, the LTC4070 is also offered in an 8-lead MSOP package. The devices are rated for operation from -40°C to 125°C.

The LTC4070 provides a simple, reliable, and high performance battery protection and charging solution by preventing the battery voltage from exceeding a programmed level.

Its shunt architecture requires just one resistor between the input supply and the battery to handle a wide range of battery applications. When the input supply is removed and the battery voltage is below the high battery output threshold, the LTC4070 consumes just 450nA from the battery.

While the battery voltage is below the programmed float voltage, the charge rate is determined by the input voltage, the battery voltage, and the input resistor:

ICHG = (VIN – VBAT) / RIN

As the battery voltage approaches the float voltage, the LTC4070 shunts current away from the battery thereby reducing the charge current. The LTC4070 can shunt up to 50mA with a float voltage accuracy of ±1% over temperature. The shunt current limits the maximum charge current, but the 50mA internal capability can be increased by adding an external P-channel MOSFET; refer to Figure 1.

Internally, the LTC4070 features a P-channel MOSFET being driven by amplifier EA (refer to Figure 2). Zero current will flow in that device until the voltage between VCC and GND reaches VF (i.e. the shunt voltage). VF can be modified by ADJ and NTC, but it is always between 3.8V and 4.2V. If the VCC voltage is below this level, then the current in the PFET is zero. If the voltage across VCC attempts to rise above VF, then current will flow in that device in an attempt to prevent the voltage from rising – this is the shunt current.

The operating current is the current required to power all of the rest of the circuitry in the chip. If no external power supply is present, then this is the current that will be drawn from the battery.

When the battery voltage is low, more voltage is placed across the input resistor, so the current into the battery (i.e. charge current) is slightly bigger than when the battery is fully charged. When the battery is fully charged, no current goes into the battery, and all of the input current goes into the shunt.

Operating current is important because is sets a lower limit on the current capability of "practical" input sources. Obviously, an input source with just 100nA of drive capability would not be able to charge a battery with LTC4070. However, with 1uA of drive capability, there is a small amount of current left to charge. If 10uA of drive capability is available, then more than 90% of that current is available for charging.

NTC Battery conditioning circuit protects batteries

The LTC4070 measures battery temperature with a negative temperature coefficient thermistor thermally coupled to the battery. NTC thermistors have temperature characteristics which are specified in resistance-temperature conversion tables. Internal NTC circuitry protects the battery from excessive heat by reducing the float voltage for each 10°C rise in temperature above 40°C (see Figure 3 for details)

The LTC4070 uses a ratio of resistor values to measure battery temperature. The LTC4070 contains an internal fixed resistor voltage divider from NTCBIAS to GND with four tap points. The voltages at these tap points are periodically compared against the voltage at the NTC pin to measure battery temperature. To conserve power, the battery temperature is measured periodically by biasing the NTCBIAS pin to VCC about once every 1.5 seconds.

Other key features

The LTC4070 has a built-in 3-state decoder connected to the ADJ pin to provide three programmable float voltages: 4.0V, 4.1V, or 4.2V. The float voltage is programmed to 4.0V when ADJ is tied to GND, 4.1V when ADJ is floating, and 4.2V when ADJ is tied to VCC. The state of the ADJ pin is sampled about once every 1.5 seconds. When it is being sampled, the LTC4070 applies a relatively low impedance voltage at the ADJ pin. This technique prevents low level board leakage from corrupting the programmed float voltage. Eliminating resistors not only saves solution size but reduces quiescent current as high-valued resistors are not needed.

The device also contains status

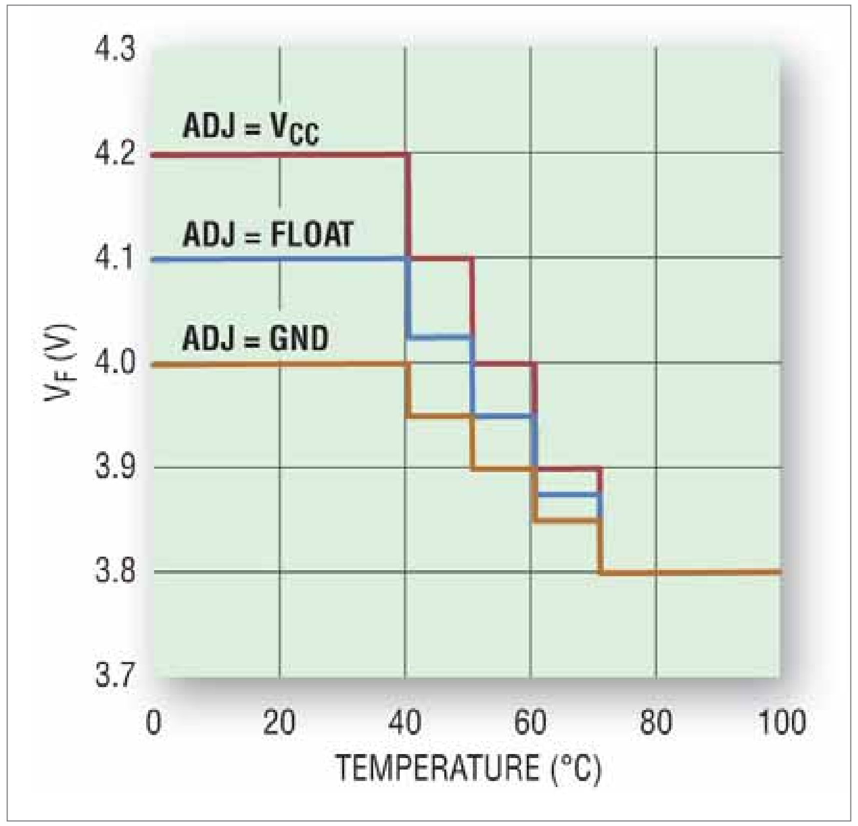


Figure 3: LTC4070 overtemperature float-voltage qualifying

outputs and signaling capability. The High Battery Monitor Output HBO is an active high CMOS output that indicates that the battery is fully charged and current is being shunted away from BAT. The Low Battery Monitor Output LBO is also an active high CMOS output that indicates when the battery is discharged below 3.2V. Finally, the external drive output pin, DRV, may be connected to the gate of an external PFET to increase shunt current for applications that require more than 50mA charge current (maximum 500mA).

Conclusion

Shunt references have many applications, and depending on their feature set, they can even be used to charge a battery. However, this type of implementation has many drawbacks including high quiescent current and lack of battery protection features. Low-power energy harvesting applications are now primed for conditioning by the right type of DC-DC converter or battery charger. Linear Technology developed the LTC4070 shunt charger system for Li-Ion/Polymer cells, coin cells and thin film batteries, to provide a simple, effective battery charging solution for cutting edge applications with low-power sources.

Author: By Steve Knoth
Senior Product Marketing Engineer
Power Products Group
Linear Technology Corporation

www.linear.com

RENEWABLES AT UNIVERSITY

A 3.3kW a-Si Photovoltaic Installation program

By PhD. Salvador Segui Chilet and Victoria Devesa

A 3.3kWpk photovoltaic installation consisting of 64 amorphous silicon modules was connected to the power grid of the Universidad Politécnica de Valencia (UPV).

The plant is located on the terrace roof of the Escuela Técnica Superior de Ingeniería del Diseño and is being used for R&D and training courses in photovoltaic installations. Several companies of the photovoltaic sector (EPVSOLAR, Danfoss, Carlo Gavazzi, Hawi, and others) participate in the project providing different materials: such as inverters, DC boxes and monitoring systems.

Installation

The 64 EPV-52 solar modules of amorphous silicon (a-Si) manufactured by EPVSOLAR are connected in 8 strings of 8 modules in series each, in a single PV array. With 20° tilt and 18.6° SW orientation the installation is done trying to reach the best architectonic integration of the PV array.

The installation is going to be used for the study of different effects and situations that typically exist in a PV installation using a-Si modules, i.e. the stabilization period, productivity under low radiation conditions, losses due to mismatching or high temperatures, among others. As it is well-known, amorphous silicon modules produce a higher energy yield per installed kWp than typical crystalline modules, even with orientations and tilt angles different to the optimal ones.

The Danfoss ULX3600 HV used in the installation is a 3.6kW single-phase inverter with a high frequency transformer and a high DC input voltage range that perfectly fits thin film module voltage characteristics. The inverter has two independent MPP-trackers and an "early start", thanks to the combination of two MPP-tracking methods, exclusively designed to work with high and low irradiation levels.

The monitoring of the PV plant is carried out by the Danfoss Web-logger with its corresponding sensors (solar radiation, ambient and module temperatures), as well as by the monitoring system developed by Carlo Gavazzi (named Eos Array), that allows to monitor independently each string of the array (voltage and current). A calibrated cell, two temperature sensors (ambient and module temperatures) and an AC energy counter with So pulses output permit the Eos Array to calculate the performance ratio of the installation and the inverter. The Eos Array is configured to store the acquired data every 1 minute, but internally it measures the values every 2 seconds and records the average value of the different magnitudes.

PV installation and control system at the University

	Jan.	Feb.	Mar.	Apr.	May	Jun.	Jul.	Aug.	Sep.	Oct.	Nov.	Dec.	Annual PSH
PVGIS	2,83	3,55	4,53	5,21	5,97	6,34	6,39	5,98	5,25	4,23	2,95	2,49	1697
Satel-light	2,79	4,18	5,00	5,84	6,21	6,68	6,93	6,43	5,29	4,40	3,30	2,62	1816

Table 1: Average daily Peak Sun Hours of each month and the accumulated yearly value according to different sources

Energy harvest

For calculating the expected energy harvest, the Peak Sun Hours (equivalent irradiance or PSH in kWh/m2•day) shown in Table 1 have been obtained from http://www.satel-light.com/ and http://re.jrc.ec.europa.eu/pvgis/ for the given conditions of the installation.

From the data supplied by EPVSOLAR, the losses due to high temperatures have been estimated accounting for a 4%. This value is significantly lower compared to crystalline modules (approximately 10%). The global efficiency of the installation (performance ratio or PR) has been estimated approximately to be 0.81, providing an energy harvest between 1357kWh/(kWpk xyear) and 1453kWh/(kWpkxyear) depending on the used PSH data. Other losses considered in the calculation are as follows: inverter losses (6.6%), conductor losses (1.5%), dirtiness (1 %), reflectance and transmittance losses (1%) and module tolerance (5%).

First results of the photovoltaic plant

With the Eos Array monitoring system the a-Si module energy harvest in cloudy days, at dawn and dusk, when the portion of diffuse light is higher and the radiation levels lower, can be more accurately evaluated. Due to the specific MPP-tracking algorithm for low irradiation levels included in this inverter, the PV plant starts producing energy already at irradiation levels of 14W/m2, with 280V on the DC side and a DC current equal to 40mA, which means 11W on the PV modules. Figure 1 shows the "early start" feature of the inverter.

Other important parameters obtained during the two first months of operation of the photovoltaic plant appear in Table 2. The measured values of PSH are close to the values used in the energy harvest estimation. The DC energy is calculated by the Eos Array using the string voltage and current magnitudes. The plant average efficiency (PR or performance ratio) during both months is higher than 90%. This value is slightly higher than the

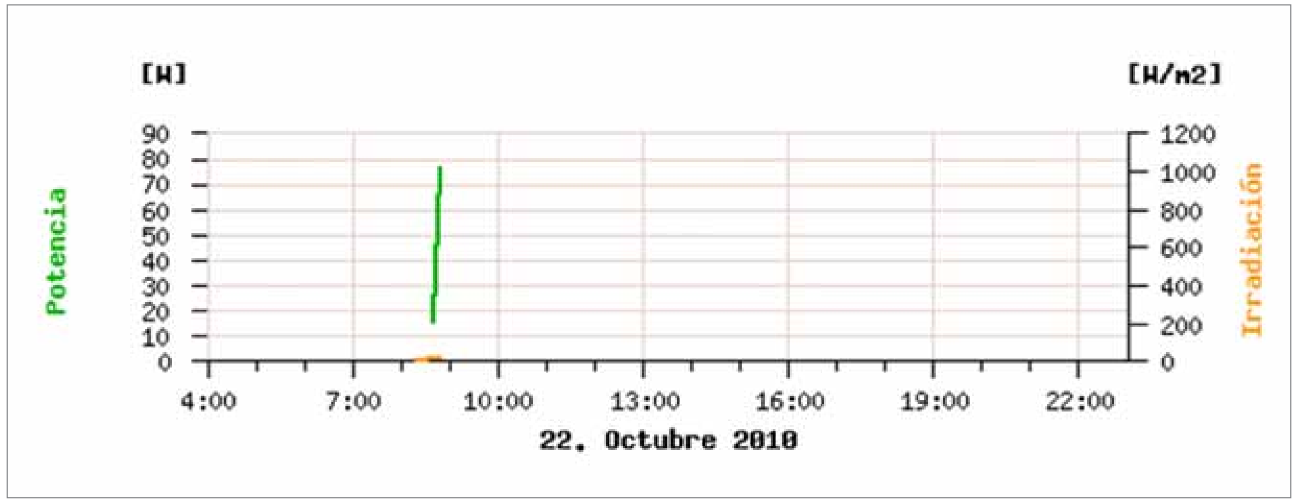


Figure 1: Power and radiation at dawn (graph from the Danfoss Web-logger)

MONTH	PSH		DC energy		AC energy		Efficiency (PR)	
	Monthly	Daily	Monthly (kWh/month)	Daily (kWh/day)	Monthly (kWh/month)	Daily (kWh/day)	Inverter	Plant
August	188,34	6,08	614,9	20,66	563,9	18,94	0,912	0,93
September	162,92	5,43	519,7	18,02	475,8	16,5	0,909	0,91

Table 2: Average values during the months of August and September

estimated one (81%) due to the fact that during the stabilization period of the amorphous silicon the rated values can be exceeded (up to 20%).

Figure 2 includes information of the daily average inverter and plant efficiencies while Figure 3 shows daily DC and AC energy and PSH. As it can be observed in Fig. 2, the inverter has reached a peak of average efficiency equal to 94.3%, with an average efficiency around 91%. The peaks corresponding to the minimal efficiencies match the days with lowest irradiation, i.e. 13/08/2010 with a total of 0.68PSH or 20/09/2010 with 1.28PSH.

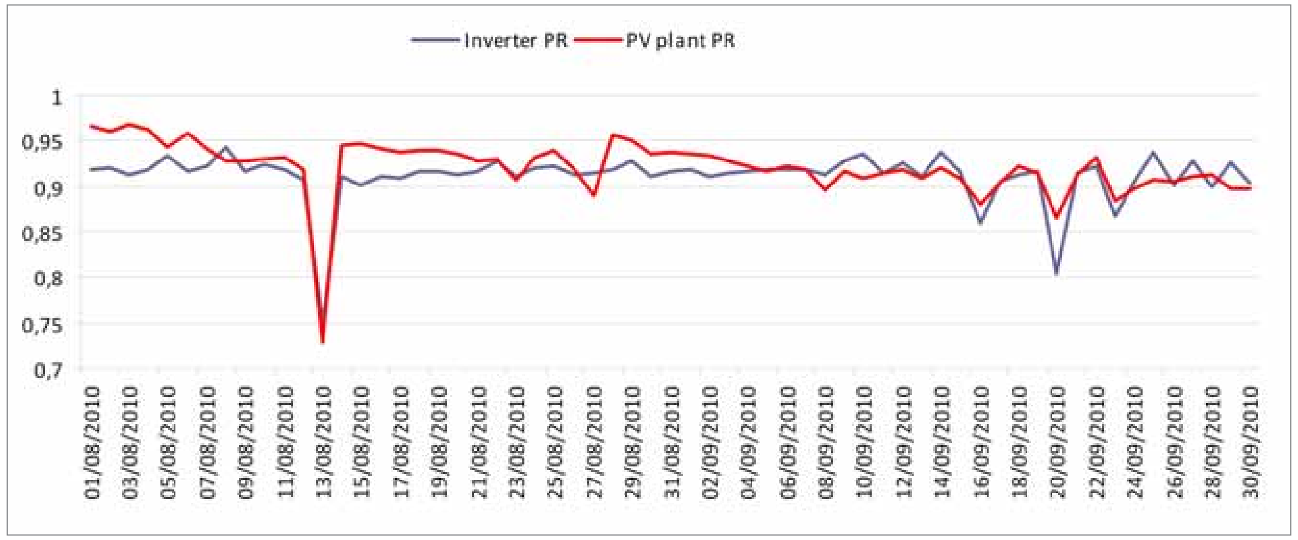


Figure 2: Inverter and plant efficiencies (Performance Ratio)

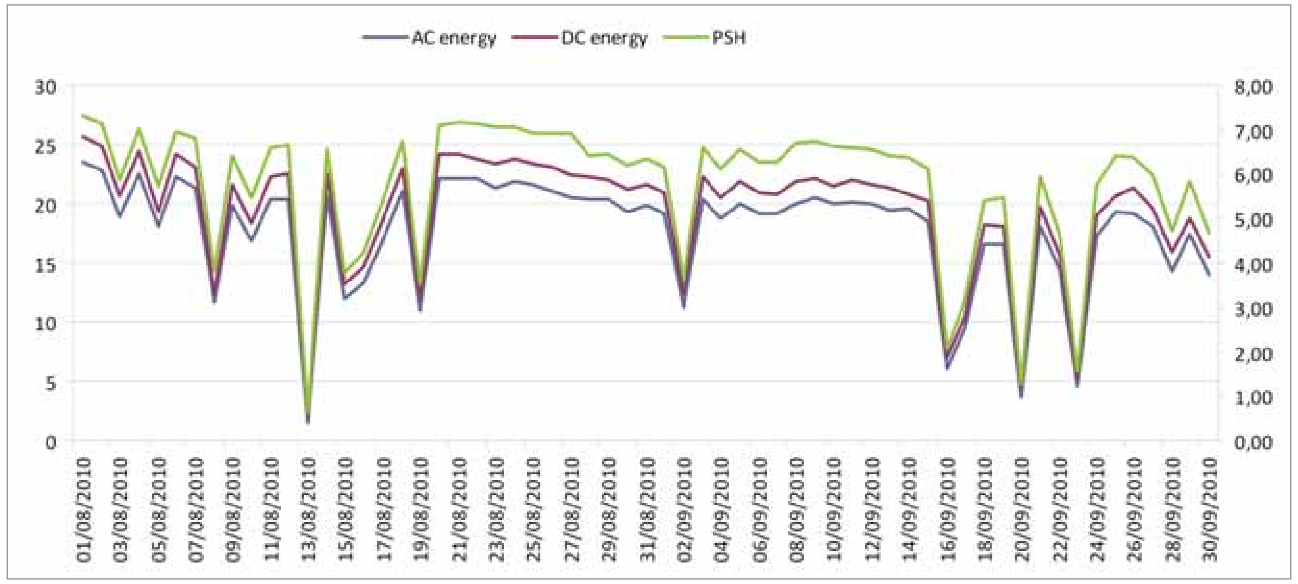


Figure 3: DC and AC produced power (vertical axis on the left in kWh), and Peak Sun Hours or PSH (vertical axis on the right in kWh/m2•day) (Measurements based on the acquired data from Eos Array)

The produced energy is fed into the power grid of the Universidad Politécnica de Valencia contributing to reduce the energy consumption of the building and becoming an example of an auto-consumption installation, still not included in the current Spanish regulation.

Future uses

In the next months, more studies concerning the performance of amorphous silicon modules are going to be carried out using the acquired information: stabilization of power, current and voltage magnitudes after the first months of operation; monthly and annually performance ratios, losses due to the effect of temperature, mismatching losses due to differences between the module parameters, etc.

This a-Si photovoltaic installation is also used during the practical parts of different training courses developed by the Universidad Politécnica de Valencia in photovoltaic power systems. The on-line course includes a virtual visit, where the student can find a complete description of all the components used in the installation as well as a video showing how the installation works. The data acquired in the installation by Danfoss and Carlo Gavazzi data loggers are used by students to analyze the behavior of this energy resource.

This photovoltaic installation clearly shows the active role of the Universidad Politécnica de Valencia in supporting sustainability and environmental concern, with the aim of increasing the public awareness about these issues, especially among internal staff and future professionals.

Author: PhD. Salvador Segui Chilet and Victoria Devesa (Universidad Politécnica de Valencia) Velencia, Spain

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PUSHING POWER CAPABILITY

Paralleling of IGBTs and diodes of one power module

By Werner Obermaier

The increasing requirement in renewable energy systems and motor drive applications for ever-higher power levels is, as a consequence, driving the demand for power modules to provide higher levels of current. The conventional approach to fulfill this requirement is to look for dedicated high current power modules, but there is another way...

This article describes the alternative approach of paralleling IGBTs and diodes within one power module to extend its power capability, for example using a 35A sixpack module as a 100A half bridge. The conclusion is that this approach provides an advantage due to the improved thermal behavior of several small chips rather than fewer big ones. The breakthrough in performance is seen when real life data of parameter variations within one power module are considered, instead of the datasheet values, which suggest a much higher spread than actually seen in real life. Figure 1 shows how a sixpack can be used as a half bridge.

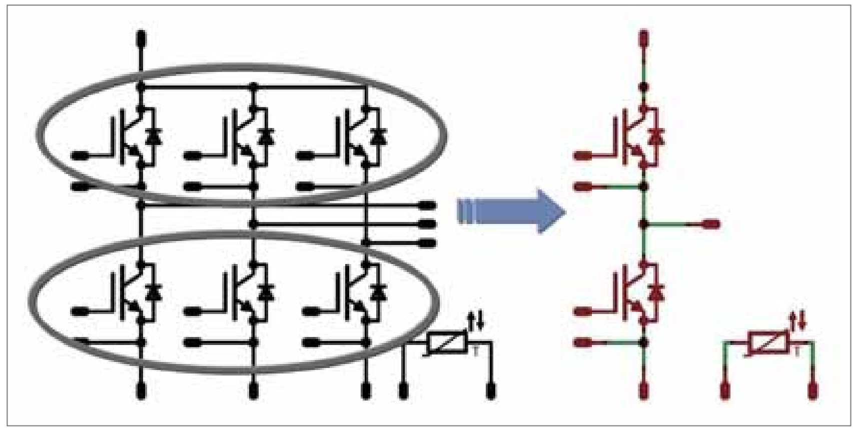
Figure 1: Sixpack Used as a Half Bridge

The following calculations are based on the P700-F sixpack module from Vincotech, which uses Infineon IGBT3 Low Loss IGBTs and Emcon HE FREDs. Both components feature a positive temperature coefficient for their voltage drop at high junction temperatures. This is important in avoiding thermal runaway of individual components when paralleled.

Switching behavior

When paralleling IGBTs, special attention has to be given to the drive circuit. Because of the variation of the gate threshold voltage of the different chips, simply connecting the gates is not adequate. Instead, each gate has to be driven by its own gate resistor and therefore it own current source in order to ensure that the chip with the lowest threshold voltage does not clamp the voltage for the others and carry all the current. Furthermore, the layout of the emitter circuit has to be very symmetrical in order to minimize differences in emitter inductances and resistances. Even minor, unavoidable differences in the emitter inductances and resistances will generate compensation currents between the gate drive emitter connections. To limit these currents, the introduction of an emitter resistance in the drive circuit is strongly recommended.

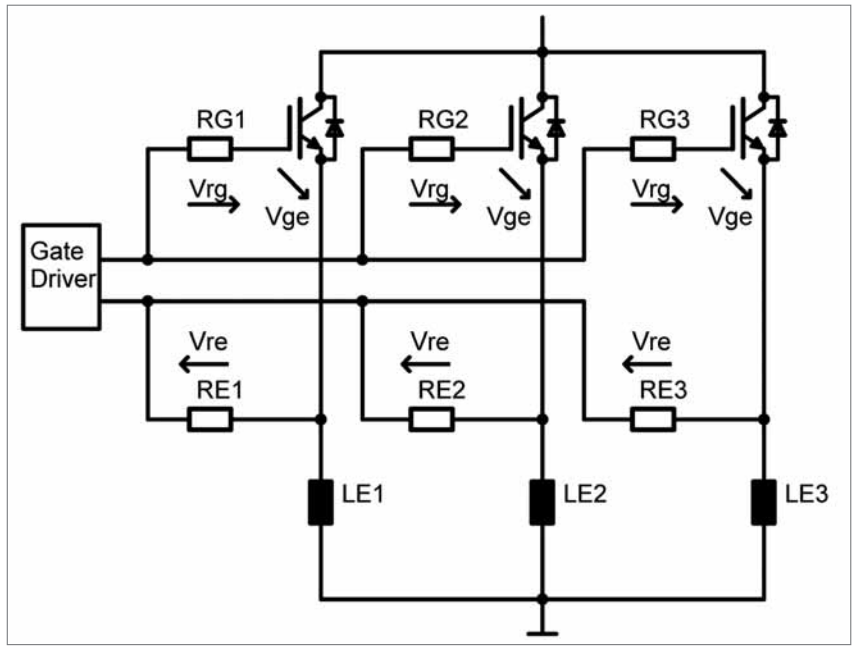

Figure 2: Sixpack Low Side with Drive Circuit

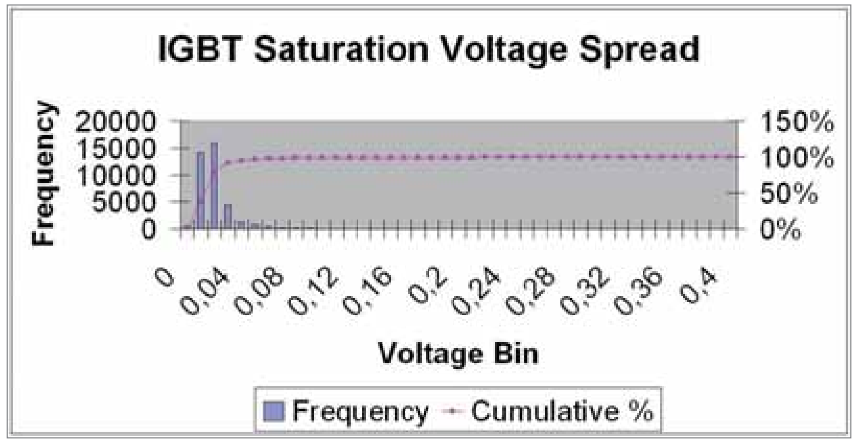

Figure 3: IGBT Saturation Voltage Spread

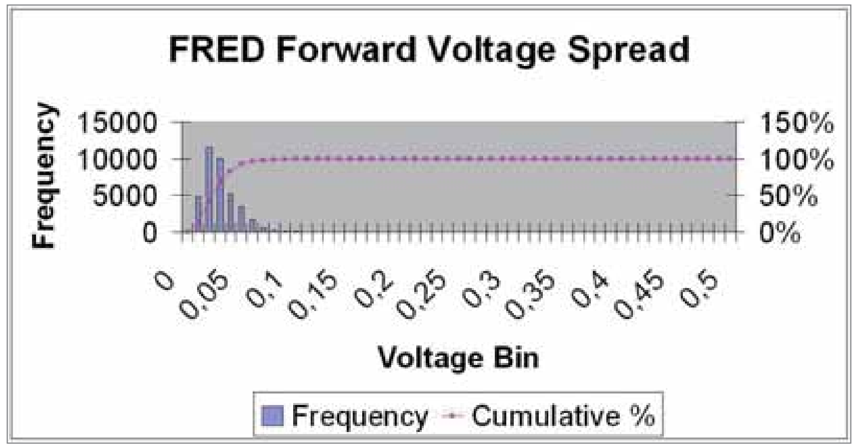

Figure 4: FRED Forward Voltage Spread

It is strongly recommended to use a resistor in the range of at least 0.5 Ohm, but not to exceed approximately 1/3 of the total gate resistance. To ensure real emitter drive sensing, the module needs to provide emitter sense connections with separate bond wires, as do the power modules from Vincotech.

Moreover, any mismatch in the delay, rise and fall times of the driver circuit are to be avoided, as these will also result in a mismatch of switching currents and therefore switching losses of the different devices. Recommended is the use of a single gate drive circuit with individual gate and emitter resistors for the different IGBTs, as shown in Figure 2. If higher drive currents are required, a single driver circuit with individual push-pull driver stages is recommended.

Since the switching losses and their mismatch depend on the layout, it is good practice to measure and confirm them in the real application. If the recommendations above are followed, it is fair to assume that the switching losses for the different devices will match to within 10 to 15%.

On-state behavior

The on-state behavior is more critical. The datasheet for the P700 sixpack suggests a relatively large variation in IGBT collector-emitter and diode forward voltage. For the IGBT, the collector-emitter saturation voltage at 25° C is given as 1.7V typical and 2.25V maximum. No value is provided for the minimum voltage. Considering this information, the paralleling of chips cannot be recommended, since the current sharing among the individual IGBTs cannot be ensured. The situation is even worse for the diodes.

In reality, however, the actual spread of the devices within one power module is much lower. This

IGBT Voltage

Probability	Voltage Spread (min/max) Tj = 25 °C	Voltage Spread* (min/max) Tj = 125 °C
99.1%	≤ 100 mV	≤ 140 mV
99.9%	≤ 240 mV	≤ 350 mV
99.99%	≤ 310 mV	≤ 450 mV

*) values are extrapolated based on 25 °C data

FRED Voltage

Probability	Voltage Spread (min/max) Tj = 25 °C	Voltage Spread* (min/max) Tj = 125 °C
99.1%	≤ 90 mV	≤ 100 mV
99.9%	≤ 200 mV	≤ 240 mV
99.99%	≤ 400 mV	≤ 490 mV

*) values are extrapolated based on 25 °C data

Table 1: Voltage Spread for Different Probabilities

is due to the fact that they are picked from locations either exactly next or very close to each other on the same wafer, and will therefore feature extremely similar electrical characteristics. To determine the real voltage variation, Vincotech has collected data from more than 40 thousand modules produced in multiple lots distributed over a period of more than one year. This evaluation shows that the saturation voltage variation for 99.99% of the high side or low side IGBTs does not exceed 310 mV at 25°C and 450mV at 125°C respectively. For the FREDs, the value is 400 mV at 25°C and 490mV at 125°C. The distribution of the voltage spread within the measured series is shown in figure 3 for the IGBTs and figure 4 for the diodes. Table 1 shows the probabilities for different voltage spreads.

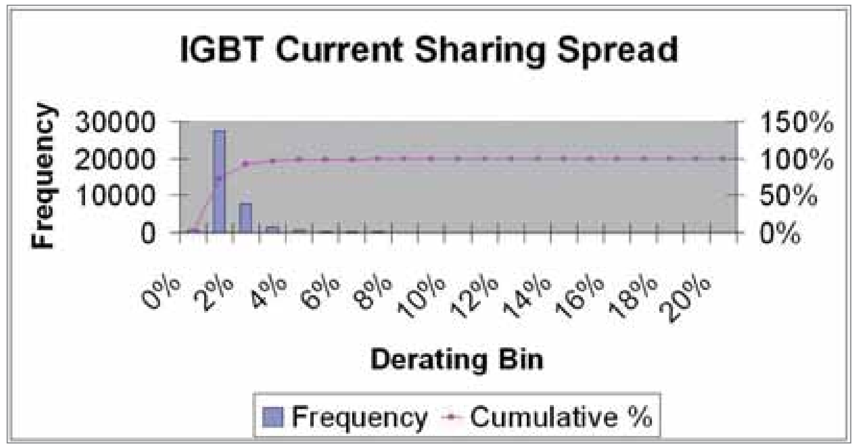

Figure 5: IGBT Current Derating Distribution

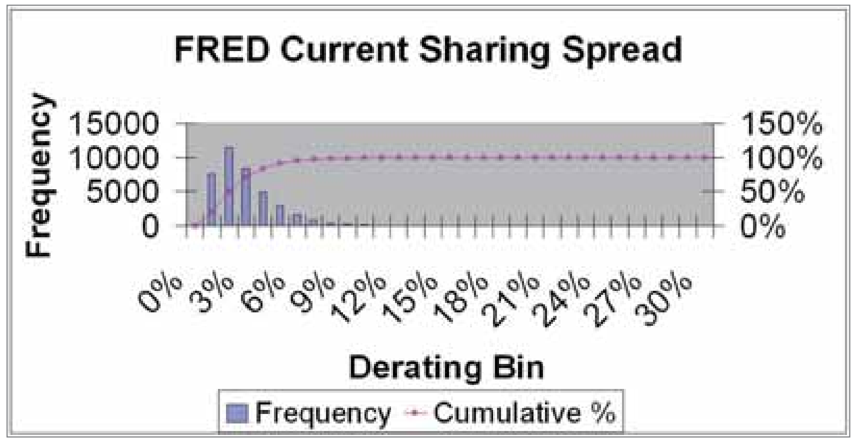

Figure 6: FRED Current Derating Distribution

When considering current sharing, apart from the low or high side of the voltage variation of the IGBTs and FREDs, it is important to know what value the third device will exhibit. Again, instead of using a worst case view based on the datasheet voltage spread, the actual data collected from the 40 thousand modules can be used. Based on this information, the current sharing can be calculated for each module individually. The device with the lowest voltage drop is used to determine the voltage for the other two devices. By doing so, it is ensured that the best device will run with the maximum current level it is designed for and that the other devices will run at a lower current level well within their design limits. The current of the other devices can be calculated using the dynamic voltage slope of the saturation voltage for the IGBT or the voltage slope of the forward current for the diode. The total current of the module can be calculated as:

$$I_{total} = I_{nom\ (best\ device)} + I_2 + I_3$$

And the current de-rating for the module can be calculated as:

$$D = I_{total} / 3 * I_{nom}$$

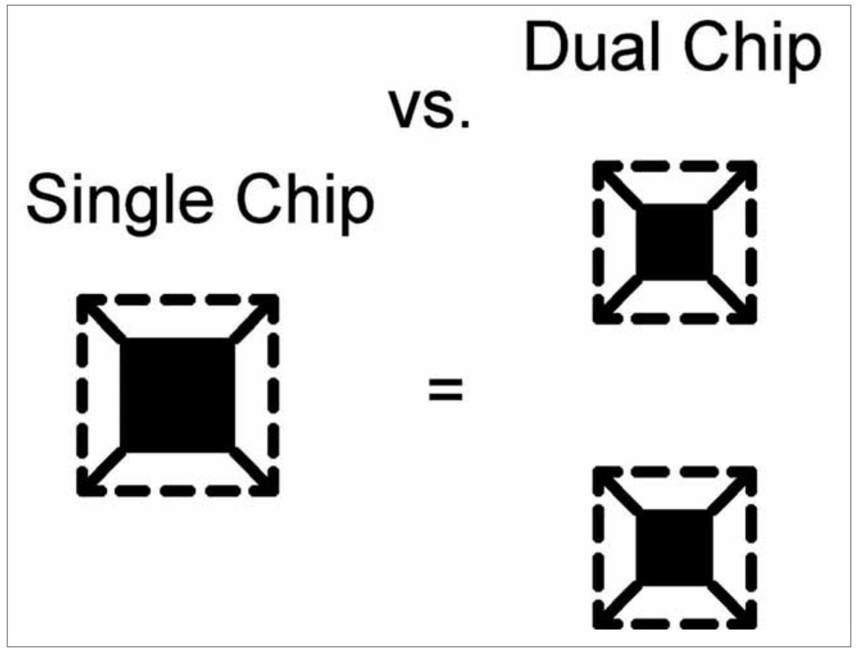

Figure 7: Improved Thermal Spreading

IGBT Current Sharing Probability

Probability	Required Current Reduction
99.9%	11%
99.99%	13%

FRED Current Sharing Probability

Probability	Required Current Reduction
99.9%	14%
99.99%	25%

Table 2: Current Derating for Different Probabilities

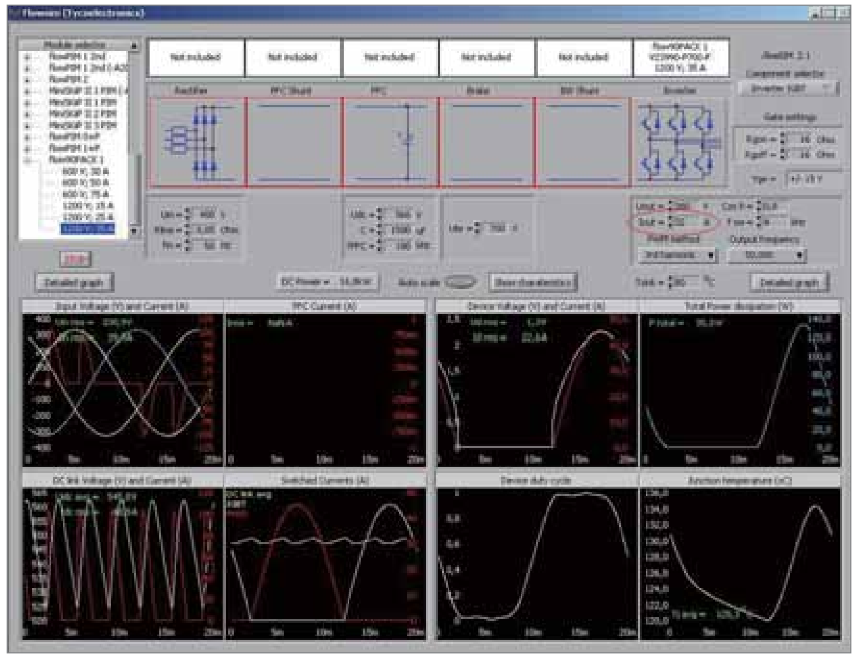

Figure 8: flowSIM P700 IGBT Phase Current Determination

Figure 5 and 6 show the distribution of the de-rating for the paralleled IGBT and FRED section of the module. Table 2 shows the probabilities for the current de-rating.

For a design where the 13% de-rating for the IGBT and 25% de-rating for the diode is used, only 1 device out of 10.000 will exceed the targeted design limit of all devices running lower than the originally targeted current. Due to this fact, this single device out of 10.000 devices may exhibit lifetime, which is lower than expected. On the other side, the distribution curves show that, for the IGBTs, 90% of the modules will share the current within 2% and 99% within 6%. For the FREDs, the current sharing for 90% of the devices will be within 5% and for 99% within 9% respectively. With a design made using the 13% and 25% de-rating, the majority of the modules will run with a much better current sharing, thus running at a temperature lower than expected. This will not only compensate for the lower lifetime of the few devices, but also improve the overall lifetime and reliability of the design.

Thermal behavior

Using multiple smaller chips instead of one larger chip improves the thermal behavior, described by the thermal impedance of a device. This is due to the fact that not only the chip itself, but also a certain area around the chip, will participate in the transfer of heat from the chip to the heatsink. Figure 7 shows the improved thermal spreading when using two small chips instead of one large, with in equal total area in both cases.

This can also be seen when

comparing the thermal resistance of the 100 A IGBT in the P569-F module with the 35A IGBT in the P700-F module. The thermal resistance junction to heatsink for the 100A device given in the data sheet is 0.57K/W. The resistance for the single 35A IGBT is 1.29K/W, resulting in an overall resistance of 0.43K/W, when 3 of them are used in parallel. This provides an improvement of about 25% in thermal performance, which compensates for some if not all of the derating required due to the non-ideal current sharing.

	P700-F		P569-F	
	IGBT	FRED	IGBT	FRED
Simulated phase current	32 A	103 A	74 A	180 A
Required derating	13%	25%	0%	0%
Resulting phase current	28 A	77 A	74 A	180 A
Number of devices	3	3	1	1
Total phase current	84 A	232 A	74 A	180 A
Limiting value for application	84 A		74 A	
Improvement	13%			

Table 3: Comparison between Single Chip P569-F and Multi chip P700-F solution

Example using 35A Sixpack power module

As an example, the performance of a 35A sixpack module used as a half bridge is compared to a 100A single chip half bridge module. The conditions and parameters used for the evaluation are shown below:

– Device:	P700:	Sixpack	35A / 1200V
	P569:	half bridge	100A / 1200V
– Motor frequency:	50 Hz		
– Cos phi:	0.8		
– PWM frequency:	4 kHz		
– Heatsink temperature:	80°C		
– Tj max:	125°C		

In the first step, the phase current capability of the individual devices, the IGBT and the FRED are determined for the P700 and P569, using the Vincotech flowSIM simulator. This simulator already takes the improved thermal performance of the smaller chips into account, which does not need to be explicitly considered later on. Figure 8 shows the flowSIM result for one 35A IGBT of the P700-F module.

In the next step, the current derating is applied and the result is multiplied by 3 for the 3 paralleled devices. Table 3 shows the result for the IGBT and FRED for both solutions.

The result reveals that the overall performance for the application at hand can be improved by 13% using the P700-F 35A sixpack instead of the P569-F 100A single chip half bridge. The actual improvement will vary for different application parameters and therefore needs to be evaluated at the most critical point.

Conclusion

The use of sixpacks as half bridges can boost the performance and enable the use of preferred modules and packages at higher power levels. Special care has to be taken regarding the drive circuit and current derating is to be considered when calculating the current of a single chip used in a multi-chip arrangement. Individual emitter sense down to chip level and symmetrical design are required of the power module, both of which are met by Vincotech modules. With the use of components in parallel, not only can higher current levels be reached, but also the reliability of the design is improved.

Author: Werner Obermaier
Head of Product Marketing
Vincotech GmbH
Germany

www.vincotech.com

POWER FROM RENEWABLES

Grid-tied PV inverter using PV-IPM

By: Cuijiao Ma, Song Gaosheng, Haitao Xiang, and Haijiang Jiang

This article describes a dual input two stage grid-tied PV inverter by using Mitsubishi Photovoltaic Intelligent Power Modules (PV-IPM) of type number PM50B6LA060. Dual circuit branches have independent boost converters and tracking control of maximum power, which can be connected with various PV arrays and make the PV system easy to use.

Small and decentralized power supplies such as used for photovoltaic generation, wind power generation, and fuel cells are in greater demand due to the rise in environmental concern. In addition, an increase in the use of domestic photovoltaic generation systems and fuel cell systems is expected in future. Because the voltage generated in these systems is DC, it is necessary to convert the DC voltage into an AC voltage for use in the home.

The device used for the DC-AC conversion is a power conditioner, and a semiconductor power device is used within such a system. High Efficiency is needed in the power conditioner, and so a semiconductor power device with low loss is requested. Mitsubishi Electric Co., Ltd has developed an IPM for the photovoltaic generation to have satisfied such a demand.

The internal circuit of a photovoltaic intelligent power module (PV-IPM) is shown in Fig.1. It integrates single phase output inverter circuit, two chopper circuits (one chopper circuit for some types and without chopper circuit for other types) and control IC into a small package. The PV-IPM adopts an innovative CSTBTTM chip technology to achieve low power loss. There is a thermal sensor mounted on the surface of each IGBT chip so that junction temperature (Tj) can be monitored accurately.

The PV-IPM has short circuit protection, control supply under voltage protection and over temperature protection. When the PV-IPM module detects overheating (OT) or load (the arm) short circuit (SC) or control supply under voltage (UV), an immediate controlled shutdown is initiated and a fault output is generated and indicated through Fo terminal.

In addition, the internal control IC can adjust gate charge according

to measured collect current in order to decrease radiation noise. A prototype Grid-tied PV inverter applying such a PV-IPM has been designed. The type name of the PV-IPM is PM50B6LA060. The structure of the system and the control approach of the grid-tied PV inverter are presented in the following paragraphs. Furthermore, the grid current and voltage based on the prototype have been measured.

Structure of the Grid-tied PV Inverter

The main circuit topology of PV inverter system is shown in Fig.2. PVa and PVb are independent PV battery arrays; L1 and L2 are boost inductors; C1 and C2 are filter capacitors; C3 is the DC bus capacitor; L3 is a filter inductor of inverter. The inverter is connected to the grid by a power frequency insulation transformer T1.

This circuit has several features. Firstly, the boost system consists of two independent boost converters which can work under various input voltage or input power to meet different requirements of customers. Both input battery boards of dual circuit branches can be mounted in different directions according to actual environmental requirements. If there is only one PV battery board, it can be connected with each of dual circuits. Secondly, the output of dual boost converters is gathered by the DC bus capacitor and connected to the grid through inverter. Finally, each boost has its own maximum power tracking control to make the system operate at the maximum power situation and improve the system efficiency.

Control Approach

The control approach of front stage boost converter is shown in Fig.3. In Fig.3, vi and vo are input and output voltage respectively; iL is current flowing through the inductor. The input reference of voltage loop control, vr is the voltage operating at maximum power and it could make the input voltage of boost inverter quickly reach the value at the maximum power situation. The converter can boost low DC voltage of photovoltaic array up to high DC voltage and transfer the electrical power to the DC bus line. The backstage inverter can keep the DC bus voltage stable by adjusting power injected into the grid. In

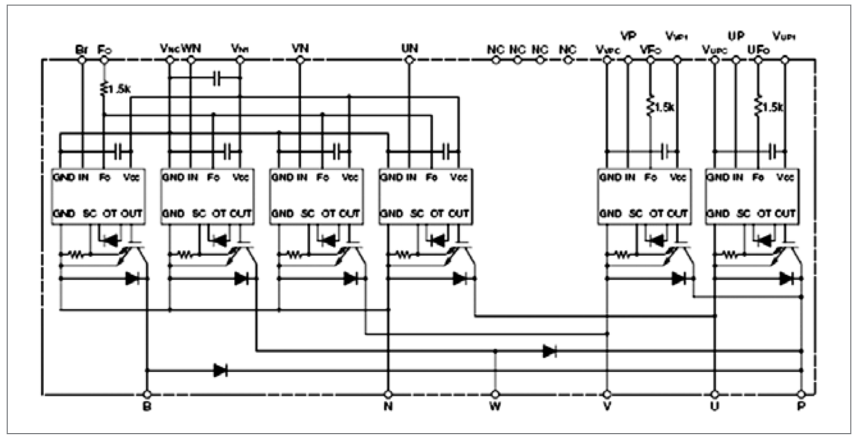

Fig.1. Internal structure of PM50B6LA060

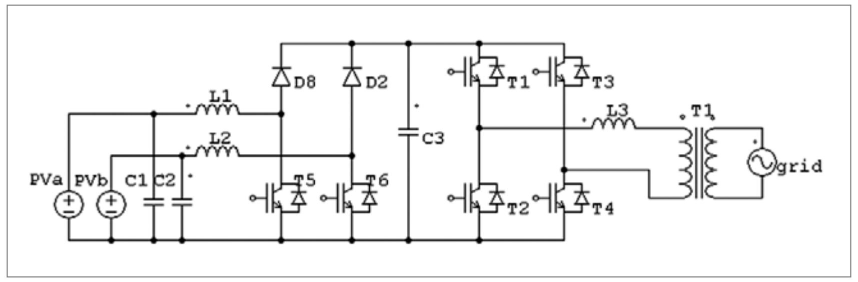

Fig.2. Dual circuit branches two stage grid-tied PV inverter circuit diagram

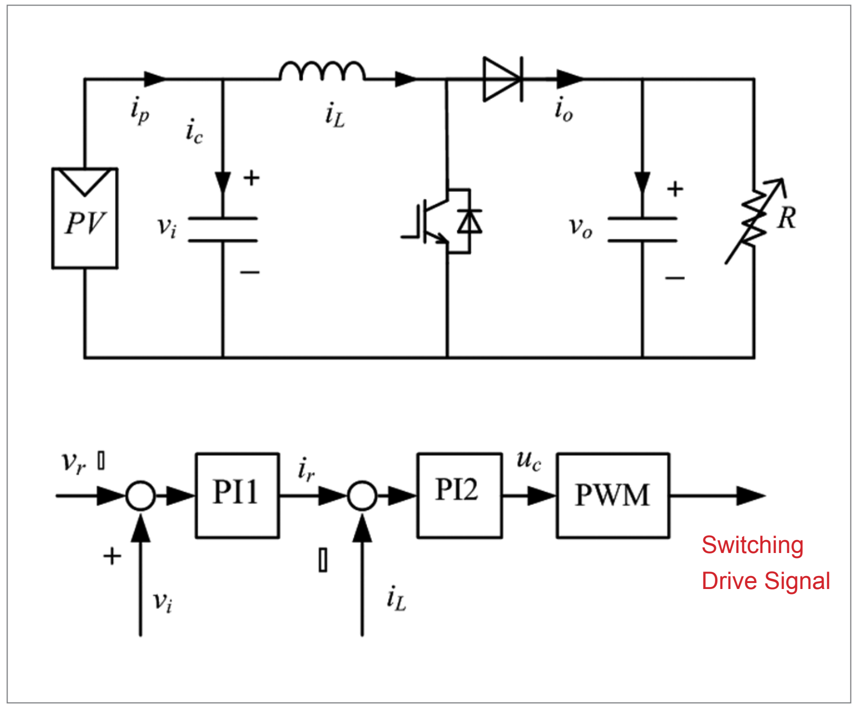

Fig.3. Boost converter and control block diagram

other words, the load of the boost converter is the DC voltage supply. The Boost converter can realize tracking control of maximum power by changing the input voltage to adjust the photovoltaic array operating points.

The backstage inverter works in current control mode. The grid-

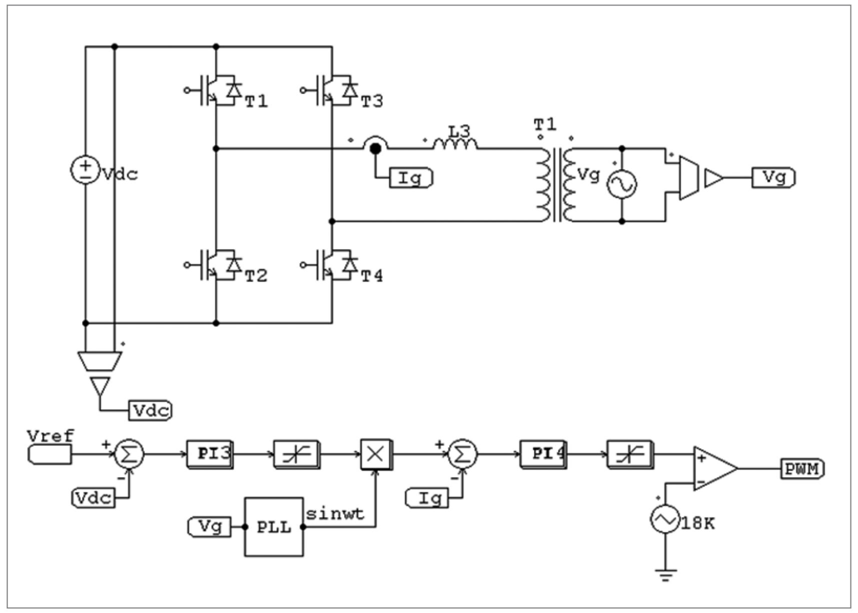

Fig.4. Inverter and its control loop

tied current or grid-tied power is dependent on the closed loop of the DC bus voltage. The control loop of the backstage inverter is shown in Fig.4. Vdc is the bus voltage and a feedback signal of voltage control loop of the back stage inverter. Vg is the voltage of the grid. The phase information of the grid voltage and reference phase of the grid current could be obtained through phase locked loop (PLL). Ig is output current of inverter and as feedback signal of the current control loop. The output of voltage control loop is the reference of grid current magnitude. However, the magnitude and the phase of the current injected into the grid are controlled by the current control loop. When the grid current magnitude is higher than the limit value, the over current protection function will be activated. This dual closed-loop control system can result that harmonic content of the inverter is lower than 3% and power factor of the inverter combined to the grid is higher than 0.99.

The power management system of the two stage grid-tied inverter is very important. The Boost converter can transfer power generated by

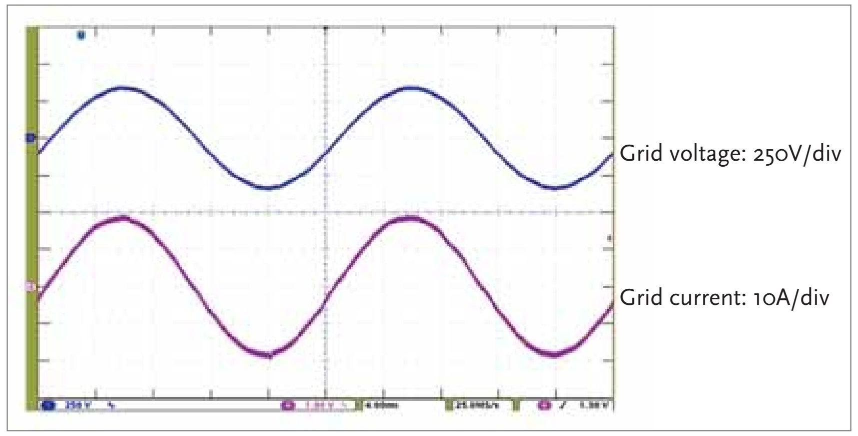

Fig.5. Test results of 3kW grid-tied PV inverter based on PM50B6LA060, full load

the PV array into the DC bus with the maximum efficiency. If the total input power from two branches is higher than the maximum output power of inverter, the inverter can be locked by over current protection to limit the grid-tied power. If the input power of DC bus is higher than output power, the DC bus voltage may rise to trigger over voltage protection. The relationship between front stage power and back stage power can be recognized by monitoring the change of the bus voltage and limitation state of the output current. The trace control direction of maximum power of the front stage boost converter is reversed to decrease the input power and keep the DC bus voltage stable when output current is on limiting situation.

Prototype of the Grid-tied PV Inverter and Test Results

Waveforms shown in Fig.5 are test results of a 3kW grid-tied PV inverter under 230V/50Hz power grid and 390V DC bus voltage. The THD of grid current in the test is 1.24%. Also, outline of the 3kW inverter and conversion efficiency versus PV voltage and power is shown in the Fig.6 and Fig.7 respectively.

Conclusions

PM50B6LA060 is convenient to be used in middle or low power single phase PV inverters with high efficiency. Dual DC input can be connected to PV arrays with different voltage and power specifications. Dual circuit branches which have independent DC-DC converters and tracking control of maximum power do not require identical input and can be easily located in a PV system. The front stage boost converters are

Fig.6. Outline of the 3kW inverter

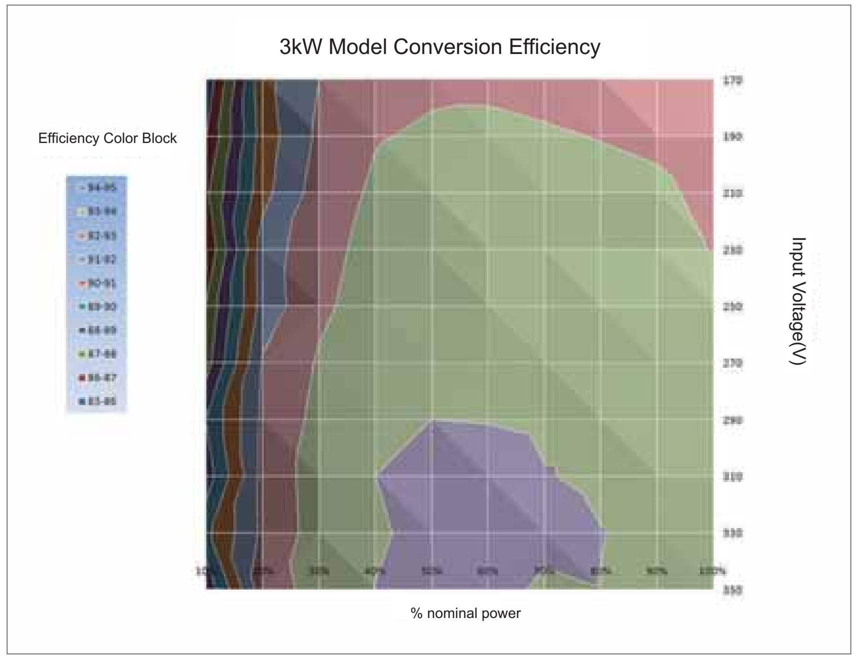

Fig.7. Conversion efficiency versus PV voltage and power

controlled independently by the same closed-loop control method and the inputs of dual circuit branches are boosted to the same bus voltage. The output power of dual circuit branches is gathered by the bus capacitor and connected to the grid by back stage inverter. The back stage inverter module is controlled by voltage outer control loop and current inner control loop. The well designed loop control system can achieve low harmonic content and high power factor. Two-stage grid-tied inverter can bring reliability to the energy management system.

Authors:
Cuijiao Ma, and Song Gaosheng
Mitsubishi Electric & Electronics (Shanghai) Co., Ltd. China;

Haitao Xiang and Haijiang Jiang
Shanghai Aero-Sharp Electric Technologies Co., Ltd. China
www.mitsubishi.com

SOLAR INVERTER INDUSTRY OFFERS TALENTED ENGINEERS THE CHANCE TO SHINE

By David Morrison

The growth in solar power is fueling sales of solar power inverters and related products, making this segment of the power supply industry one of the most vital and dynamic. According to iSupply, shipments of solar inverters worldwide are expected to climb from 2.6 million units in 2010 to over 23 million units in 2014.

This corresponds to an increase in sales from $5.3 billion to $8.9 billion over the same period. Meanwhile, a report from IMS Research that focuses on the market for microinverters and power optimizers, predicts that suppliers of these products will ship more than 16 million of these products over the next five years with these sales accounting for over $1.5 billion in revenue.

As solar power inverter manufacturers gear up to meet these demands, many are expanding their engineering teams through hiring of additional power electronics (PE) engineers and other electrical engineers (EEs). A recent survey of vendor websites found openings for power electronics engineers at numerous companies in this field including Enphase Energy, Schneider Electric Renewable Energies, Power-One, Petra Solar, Danfoss Silicon Power, SolarBridge Technologies, and Eltek Valere. (You can view these job postings in the online version of this article.) Manufacturers are looking for both new graduates and experienced engineers with strong theoretical and practical knowledge of power electronics, including the latest digital control techniques. When evaluating experienced candidates, they also value those who have designed power systems for high-reliability applications. Competition for good candidates is said to be very strong due to competition within the solar inverter industry and from other industries. This factor combined with the strong growth of the industry, the technical challenges, and the opportunity to further the development of renewable energy, may make the solar inverter industry attractive to many power electronics engineers as well as to EEs who have other skills needed to develop inverters and related products.

Model Candidates Have Bench Skills Too

Companies that build solar power inverters often need a mix of experience levels, ranging from recent university graduates with masters and PhDs from power electronics programs, to engineers with years of industry experience. This is true at companies such as Enphase Energy and Eltek Valere. Enphase makes micro-inverter systems primarily for residential and commercial applications. Meanwhile, Eltek Valere makes string inverters for residential and small commercial or industrial applications as well as central inverters for larger industrial applications such as power plants.

Whatever their level of experience, candidates are expected to be well versed in the fundamental analog and digital aspects of power electronics, and have strong simulation and bench skills.

"We're looking for people with very good analog skills and lots of simulation background," says Mark Baldassari, director of Hardware Engineering at Enphase Energy. "Our systems are digitally controlled [even in the control loops], so we're looking for digital control theory or practice."

Ingvar Apeland, VP of renewable energy at Eltek Valere, also notes the importance of digital control in describing the ideal candidate for PE design positions. He explains that candidates are expected to have experience with "DSP-controlled electronics and experience with inverter technology and advanced power electronics technology."

A background in simulation is important, but not sufficient in itself. Baldassari explains that candidates "must have experience validating their models and their simulations. You can simulate whatever you want but it has to work in the lab."

Baldassari says that even recent graduates must have some degree of lab experience—something candidates can expect to be asked about in interviews. When interviewing new engineers, Enphase expects them to discuss the work they've performed at the university in a way that demonstrates they truly understood what they were designing, and were not simply part of a design team. The goal says Baldassari is to find "the top graduates from the universities."

Once hired, recent graduates need to gain practical experience by working under the more-seasoned engineers. But even as they are being trained, there are contributions that new engineers can make right away. This is particularly true for those who have just completed PhD programs in power electronics. Baldassari notes that these engineers arrive with valuable training in simulation.

"We look at the new college grads to bring that into our company because they're up on the new tools. They've also had access to many tools that might be quite expensive, maybe even too expensive for us to afford. But recent graduates have that experience and that level of knowledge," who adds the caveat "as long as they've done some model validation along the way."

When seeking experienced PE engineers both Baldassari and Apeland make it clear that the goal is to find extremely well qualified candidates.

"The challenge is not to find the volume of people, the challenge is to find the absolute experts in their field, the top people that you can grow the rest of your team around. That is always the challenge and always a critical success factor for any R&D environment," says Apeland.

Design for Reliability Counts

Companies such as Enphase and Eltek Valere do hire engineers who have worked at other inverter and traditional power supply companies. But this isn't a pre-requisite by any means. Candidates for PE engineering positions won't be expected to know the specific solar power application requirements—this is something their employers can teach them.

"They could be from the solar inverter industry or also from a related industry," says Apeland. "It's not necessary that they have developed solar inverters before."

This makes it easier for solar inverter companies to hire engineers from other industries such as military/aerospace or automotive. Engineers coming from these industries may be particularly attractive to solar inverter manufacturers because these others industries also stress design for reliability, which is critical in the solar power market.

"We try to design and develop a very reliable system, so we find that the military experience is also a good background because there, high reliability is the key," says Baldassari. "But at the same time we have to temper any design with cost because we're in a very competitive market," he says, adding "We need satellite performance at laptop prices."

Candidates from the automotive industry are also of interest because of that industry's focus on reliability. The telecom/datacom industry is another that shares a concern with reliability. Although today this industry is not the source of power electronics engineers it once was, Baldassari notes that the founders of Enphase came from the telecom/datacom world in which five-nines reliability is a crucial issue.

While power electronics engineers

are at the core of any solar inverter design team, the companies also need EEs with other skills and backgrounds. Some of these EEs are needed to develop the hardware and software that companies offer to support the operation of the inverters and related products.

"We're also looking for communication engineers to help us out with our power line communications. We look for mixed-signal engineers [including ASIC designers] that have digital and analog experience for products such as our communications gateway device, consumption monitor, smart meter, smart thermostats, and other peripheral devices that we want to develop," says Baldassari.

Similarly, Apeland notes Eltek-Valere's need for other types of non-power specialists. "We also use people who don't have exactly power electronics background, but more software and controls and other types of electronics experience," says Apeland. "It depends on how you put the teams together and what other experience is needed in the same team."

EEs with other backgrounds also support product development functions such as test automation and standards compliance. Compliance engineers keep track of safety, EMI and other specifications required for photovoltaic systems in various markets and help inverter design teams to develop different inverter models to meet the different market requirements. Engineers working in these peripheral areas of inverter development may not be expected to have a power background, but it is considered a plus when they do.

About the Author

David G. Morrison is the editor of How2Power.com, a site designed to speed your search for power supply design information. Morrison is also the editor of How2Power Today, a free monthly newsletter presenting design techniques for power conversion, new power components, and career opportunities in power electronics. Subscribe to the newsletter by visiting www.how2power.com/newsletters.

Author: David G. Morrison
Editor
How2Power.com

www.how2power.com

GREEN SUN

By Cliff Keys

With the industry focus on renewable energy sources, power engineering - and in particular, energy harvesting and the constant quest for the highest efficiency, looks set to maintain significant growth in the foreseeable future. This should prove to be a boost to our industry.

Moore's law in solar market

Because of their capability to bring the beneficial dynamics of Moore's Law to the solar market, global shipments of PV Module Level Power Management (MLPM) systems are set to explode during the coming years, according to iSuppli. Global MLPM installations are forecast to reach 7.8GW by 2014, managing a Compound Annual Growth Rate (CAGR) of 204.3%, up from just 30MW in 2009.

The Silicon Valley mantra of smaller, faster, cheaper hasn't really applied to the PV market until recently, when MLPM systems started being employed in solar installations. Rather than reducing costs the way microchips do - by becoming smaller and faster - PV systems historically have achieved the 'cheaper' part of the equation by delivering on the three efficiencies of solar technology: efficient energy conversion, efficient manufacturing methods and efficient use of materials. However, the PV market is beginning to take a page from Moore's Law with the arrival of MLPM systems.

Sun harvest

MLPM systems are beginning to gain favor because of the increased energy harvest that they enable at the individual module level, instead of at the total module string level. Depending upon the location of installation, such as "shadowing" conditions, MLPM solutions can harvest 3% to 20% more kilowatt hours of PV electricity during the course of a year. And while they cost significantly more per watt than traditional inverters, that gap is rapidly narrowing.

Micro-inverters perform the same general functions as traditional inverters except that they work on a per-module basis rather than for a string of modules. Optimizers perform the Maximum Power Point Tracking (MPPT) algorithm and are often used in conjunction with a string inverter that has been cost-reduced by removing the MPPT function.

Applying Moore's law

The Bill of Materials (BOM) for MLPM systems are more chip intensive than that of regular inverters. Micro-inverters also are adopting some of the latest advanced semiconductor technologies, such as Gallium Nitride (GaN) power components.

Being chip intensive is actually helping these systems by allowing them to drive out costs, as they benefit from functional integration and the lower power draw from the constantly evolving chip-process technologies.

The use of chips is also allowing MLPM system providers to offer much longer lifetime warranties than traditional inverters, to 15 years and beyond, which more closely aligns with the payback lifetime of PV installations.

It remains to be seen how much regional governments and administrations will be actually prepared to invest in the training of engineers and the support for this industry, certainly they have fully exploited it as a vote-catcher.

Author: Cliff Keys
Editorial Director & Editor-in-Chif
Power Systems Design
www.powersystemsdesign.com