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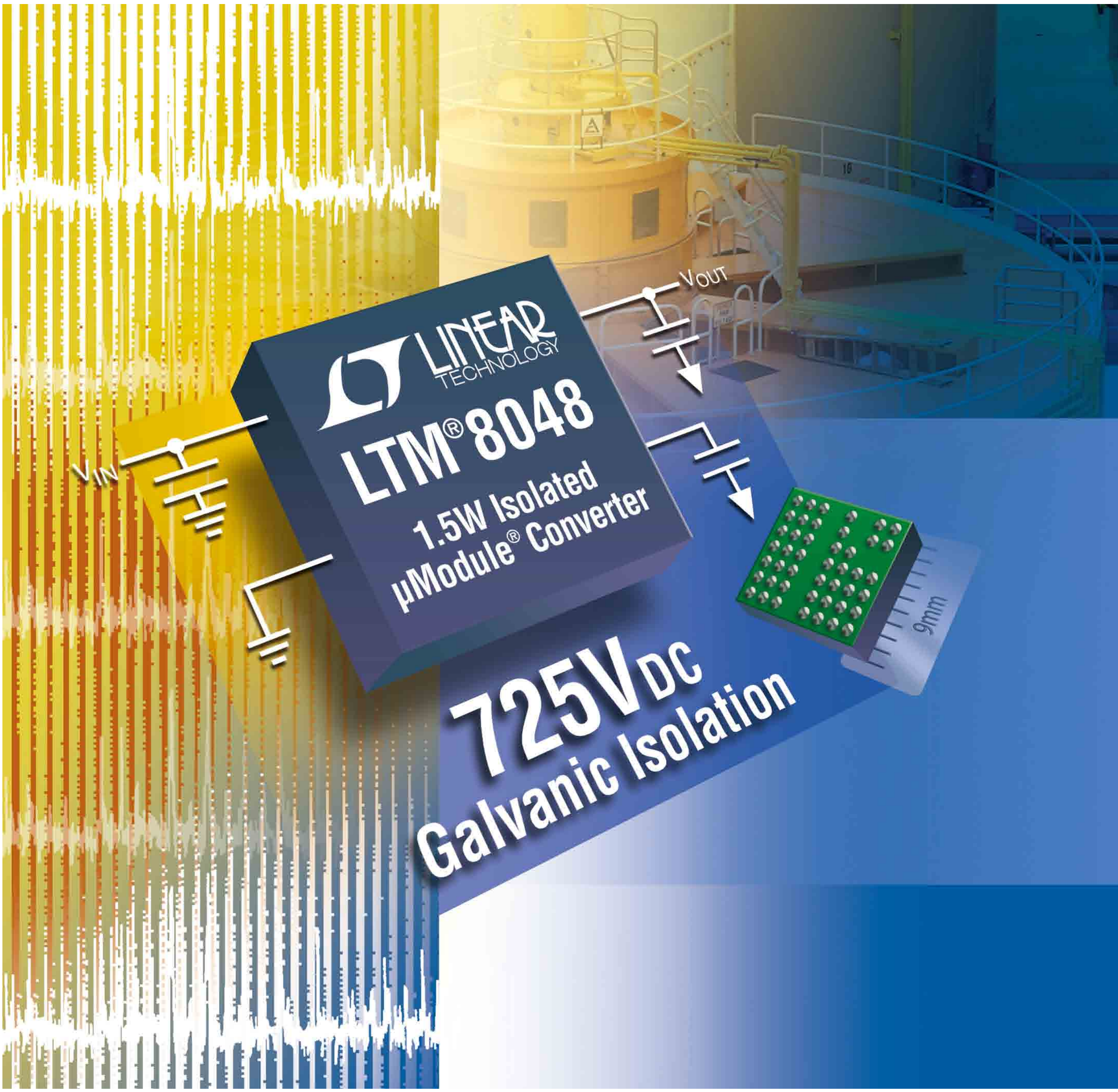
January/February 2012




SPECIAL REPORT: RENEWABLE ENERGY (PG29)

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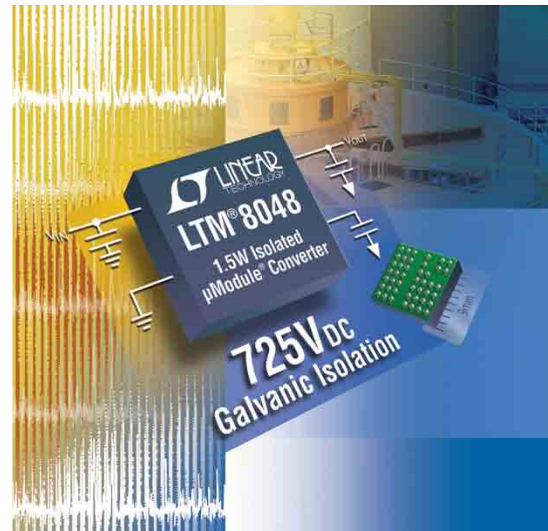


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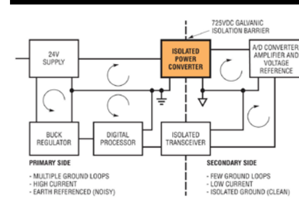

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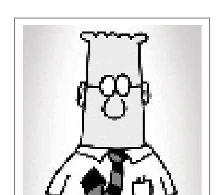

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# EFFICIENCY: AN ENGINEERING TASK

Our January-February issues of Power Systems Design Europe and North America run with the theme 'Energy Efficiency, Test and measurement'.

With the future of our traditional energy resources depleting and the concern over the condition we leave our planet in for our children, energy efficiency has never been so important. Companies are desperately telling their engineers to reduce power levels - a tough call that only our worldwide engineering community can fix.

All designs for electronic equipment now have this as a major consideration and power has never been such an important part of the design process. Technology, in this respect, is moving so fast that half the problem for the designer is in finding and selecting the right technology and components.

In this issue I wanted to explore, at all levels, the current and future advances in the power electronics industry. We now have Silicon Carbide (SiC) and Gallium Nitride (GaN) at our disposal as real products.

The global power semiconductor market is predicted grow by just 5.0% in 2012 to $32 billion, according to IMS Research which has cut its previous forecast of more than 8% due to global economic uncertainties and inventory being flushed from the supply chain. The market, which grew by 37% in 2010, is however forecast to return to double-digit growth in 2013. Latest findings from the company's Power Management Quarterly Market Watch revealed that the power semiconductor market (including power discretes, power modules and power ICs) grew by just 3.7% in 2011, following its strong recovery in 2010. Whilst demand remained relatively robust in the first half of 2011, inventory corrections and major economic uncertainties surrounding the Euro-zone crisis resulted in declines in Q3'11 and Q4'11.

The power IC market growth was almost 3% lower than power discrete growth in 2011, though this trend is set to be reversed in 2012, with slightly higher growth predicted for power ICs. The power module market continued to outperform both power discretes and power ICs, showing sustained high double-digit growth in 2011, which is projected to remain in for the next four years, driven by demand for IGBT modules.

Whilst factors such as inventory correction resulted in a slowdown in demand in 2H'11, particularly for power discretes and power ICs, growth projections for 2012 are more directly linked to end-equipment demand. This demand, however, also differs largely by application.

I do hope you enjoy this issue of the magazine and please don't forget to check out Dilbert at the back and keep the feedback coming in. I appreciate this.

All the best

**Cliff**
Editorial Director & Editor-in-Chief
Power Systems Design
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# IR's TRUE DIGITAL POWER SOLUTION

International Rectifier has announced that its digital power solution featuring GUI-based VR design for fast, real-time tuning and system-level optimization powers All New 3-Way Digital X79 motherboards from GIGABYTE™, a leading manufacturer of motherboards and graphics cards.


"As a pioneer in the manufacture of motherboards and graphics cards, we embraced the leading-edge true digital power solution offered by IR. We were able to implement an extremely high performance overclocking feature set using IR's unique range of technologies. As a result, IR's easily implementable, highly efficient and effective system-level solution was exceptionally well suited to our all digital 3D Power™ X79 Series of motherboards," said Henry Gao, Vice President of the GIGABYTE Motherboard Business Unit.

"As demonstrated by this new high performance X79 Series, IR's true digital power platform offers significant system-level benefits to GIGABYTE and their customers. We engineered enormous flexibility and superior voltage regulation into our controllers, allowing GIGABYTE and their customers to overclock these newest complex processors and DDR memory to levels that were not possible with analog or hybrid digital control," said Deepak Savadatti, Vice President and General Manager, IR's Enterprise Power Business Unit.

Featuring Dynamic Phase Control (DPC) and Variable Gate Drive (VGD) technology, IR's true digital solution enables more efficient delivery of power to the processor over the entire load range to enhance system performance and end-user experience. IR's CHiL digital controller eliminates many external components necessary using hybrid digital or analog controller solutions to offer an extremely small, high density solution that allows incremental space on the motherboard to add extra system-level features.

The IR digital platform features a non-linear control architecture (adaptive transient algorithm, ATA) to allow best dynamic response with reduced output capacitor count to keep up with the demanding and highly variable workloads of the processor. Its true digital engine allows superior on-the-fly performance optimization across the full operating range and even above the range of the processor without the need to modify hardware, while maintaining fully stable operation. The solution also provides a full suite of telemetry via built-in I2C digital interface to offer real-time monitoring of voltage, current, temperature and power to fully optimize and maximize power delivery to the processor.

More information is available on the International Rectifier website at:

www.irf.com

# BOOSTING ENERGY EFFICIENCY IN POWER CONVERTERS

By Stephen Oliver

From lossy DC distribution buses in telecom equipments to power hungry datacenter servers and emerging aerospace systems, the quest to further cut power losses and improve the overall efficiency of power solutions in these applications is very high.

Although, the traditional AC-DC silver boxes have evolved into distributed power architectures, which have further migrated to intermediate bus architecture (IBA), in telecom equipments, server boards, and aerospace systems, to raise the efficiency bar, they have now reached a plateau. And the issue is more evident when the point-of-load (POL), such as the processor voltage on the motherboard drops below 1 V. In fact, the overall efficiency drops.

The move to higher DC bus voltage (48V or 350/380V) reduces the distribution losses but adds an extra stage of DC-DC conversion to get down to the intermediate voltage of 12 VDC before powering the low POL voltage with synchronous buck regulator, resulting in bigger size and lower conversion efficiency.

To overcome the limitations of high voltage distribution bus, European standards agency ETSI is working on a new standard, +/- 190 VDC. The recent transition from 380 V DC bus voltage to +/- 190 V for the telecom DC distribution lifts the efficiency bar again. However, using the new ETSI bus voltage standard also requires additional conversion stages as shown in Figure 1. Here again, the +/-190 VDC is converted to 48 VDC, which is then lowered to 9.6 or 12 VDC using the IBC. The efficiency gain is negligible, while it adds more components to reduce power density and increase overall cost of the solution.

Vicor prefers combining efficient power components with an optimized architecture in a holistic approach. For that, the company has developed highly efficient modular building blocks called V.I Chip, which can be combined with an optimized architecture like the factorized power architecture (FPA) to surmount the drawbacks of traditional high voltage rails, including the new ETSI standard, in telecom equipments, servers and aerospace systems. In essence, it can deliver power solution with unprecedented combination of power density, efficiency and flexibility.

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*Andover, MA*

# 2011: A YEAR OF TWO HALVES FOR POWER INDUSTRY

By Ash Sharma

2011 was certainly a year of two very different halves. The first half of course started strongly, building on the momentum that 2010's recovery had brought.

Power component companies certainly felt the effects of this tumultuous year. First half power semiconductor revenues exceeded $15bn; however, this was then followed by two quarters of declining revenues. Despite this weaker second half, 2011 was still a positive year for the power semiconductor industry. Power discrete revenues grew by 3% over the prior year.

Power IC revenues were broadly flat, whilst the power module market grew by nearly 18%. IGBTs and MOSFETs were the main drivers of growth for the discrete market. The automotive, industrial and lighting sectors all stood out as the most rewarding markets for power discretes last year, though this may well change in 2012. IGBT products also drove the majority of power module revenue growth in 2011 and exceeded $4bn for the first time. For the power module market, booming sales of motor drives was the key factor behind its impressive growth. Solar inverters which had previously been an important growth driver for power modules weakened considerably in 2011.

2012 is likely to be another year of two very different halves for the power semiconductor market, starting with a weak first six months and finishing with a stronger second – although the global economic outlook is yet again very uncertain. Many major countries' governments are still grappling with burdening sovereign debt issues and many of these countries look to be heading back into recession. Customers are continuing to tighten their belts resulting in what's projected to be a flat 1H (over 2011). Assuming the Euro-zone crisis gets resolved without any further significant fallout, we predict more robust sequential growth to resume in Q3 and quarterly power semiconductor revenues will rise above $8bn for the first time on record. However, total growth for the year is forecast to be just 5% in 2012, much lower than the historical results.

The underlying factors behind the power component industry's growth still remain very positive however. Almost every end-sector now has an increasing focus on energy efficiency and energy savings which will help to continue to drive investment and growth for power components. Growth is not simply determined by increases in consumer and commercial spending and is likely to outpace growth of other component markets. Manufacturers may well experience a difficult and unpredictable 2012, but should take solace as double-digit growth is predicted to return to the industry in 2013 and the future remains positive.

*Author; Ash Sharma*
*Senior Research Director*
*IMS Research*

www.imsresearch.com

# FLYBACK TRANSFORMER PRIMARY WINDING STRUCTURES

By Dr. Ray Ridley

Dr. Ridley shows how the intricate details of magnetics construction can have a major impact on the operation of a flyback converter.

**Flyback Transformer Primaries**

If you are designing a flyback converter, it is normally for a high-voltage input, and you do not need a lot of power – typically 10 watts or less. Space is always at a premium, and you want to keep the transformer as small as possible.

These common constraints often lead to a design with a small core, and many primary turns, often more than 100. The use of multiple winding layers cannot usually be avoided, and a decision must be made about exactly how to arrange the multiple layers of the winding. In this article, the case of a 130-turn primary, wound in two layers on an EPC19 bobbin from TDK will be considered. Three different winding configurations were built and tested.

Figure 1 shows the first configuration, where a 34 awg wire is wound out and back across the bobbin with no tape between the layers. This is the most common arrangement since a low-cost winding machine can be programmed to automate this layout very easily. It is also very easy to build manually for prototyping.


*Figure 1: Flyback Transformer Two-Layer Primary with No Tape. This is the Maximum Capacitance Configuration.*

Unfortunately, this is also the worst way to arrange a two-layer winding since it produces the maximum winding capacitance, and the maximum voltage stress between adjacent wires at the beginning and the end of the winding. Despite these drawbacks, most manufacturers wind this way, and most designers do not have the experience to insist on changes that can improve the performance.

Figure 2 shows the frequency response measurement of this transformer primary winding configuration. All measurements in this article were made with the AP300 frequency response analyzer, configured to measure high impedances, and transformer capacitances as low as 2 pF.

From this frequency response curve, the inductance of the primary winding is calculated at 100 kHz to be 67 μH. The first resonant peak in impedance

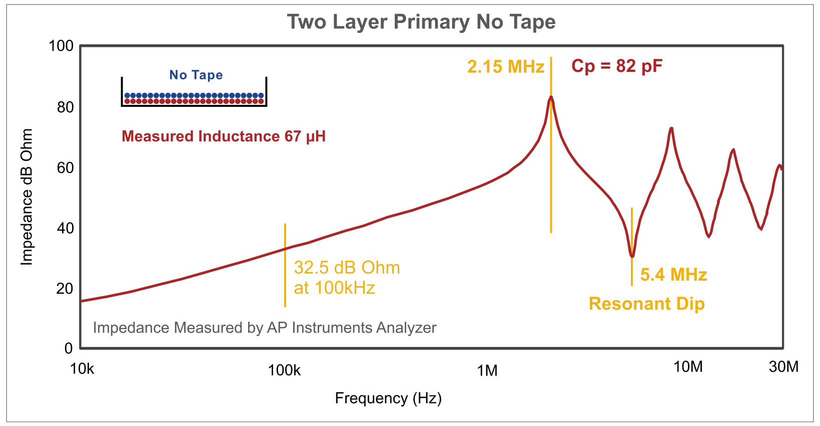


*Figure 2: Primary Impedance Measurement with Maximum Capacitance Winding Configuration, Two Layers with No Tape. Equivalent Capacitance is 82 pF.*

occurs at 2.15 MHz, and this corresponds to a primary capacitance of 82 pF. While this may seem like a small value of capacitance, it will cause a significant leading-edge spike on the current waveform in the flyback primary.

The winding arrangement also gives a dip in impedance at 5.4 MHz, and this sharp dip will result in ringing of the primary current. Both the leading-edge spike, and current ringing are shown clearly in Figure 3.

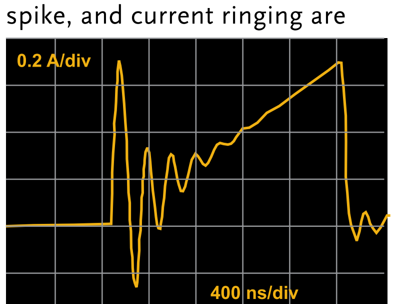


*Figure 3: Primary Switch Current with Maximum Capacitance Winding. Notice Large Initial Current Spike and Continued Ringing. Frequency of Ringing Corresponds to the Resonant Dip in the Impedance Measurement.*

Waveforms like this are quite common in production power supplies. However they present problems of EMI, current-limiting precision, and protection. The waveforms can be improved by some simple changes to the primary of the transformer winding.

**Flyback Transformer Primary with Tape Insulation**

The high capacitance of the configuration of Figure 1 results from the very thin insulation on the windings, and the close proximity of windings with high voltage differentials. The performance of the winding can be improved by placing a layer of tape between the two layers of wire, as shown in Figure 4.

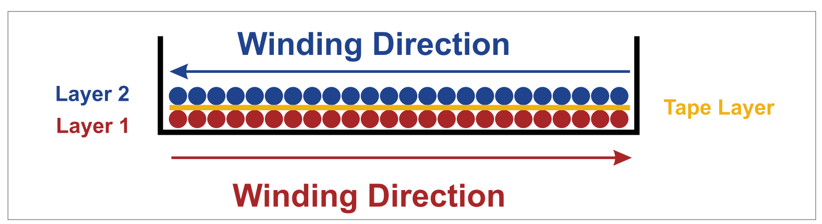


*Figure 4: Flyback Transformer Two-Layer Primary with Layer of Tape.*

A more sophisticated winding machine is required to add the layer of tape, and some manufacturers may be reluctant to make this change. However, the advantages are significant, as shown in the frequency response measurement of the primary impedance shown in Figure 5. The calculated primary capacitance is reduced by more than three times with the introduction of the tape between the windings. The design is also more rugged with insulating tape between the highest voltage windings, and less likely to fail from voltage breakdown over the life of the power supply.

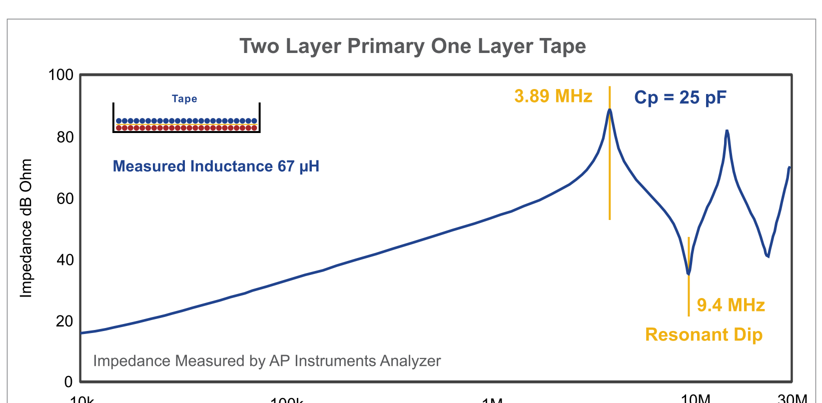


*Figure 5: Primary Impedance Measurement with Layer of Tape Between Winding Layers. Equivalent Capacitance is 25 pF.*

While the waveforms will be improved with this winding layout, even more can be done, as shown in the next section of this article.

**Segment-Wound Primary Winding**

High-voltage transformer designers commonly use a segmented winding technique to optimize the performance of high turns-count windings. This has many significant advantages, including:

1. Reduction of capacitance
2. Reduction of voltage stress on adjacent turns. This is essential for kV application in order to avoid corona.
3. Automated winding with an appropriate winding machine.
4. Use of more conventional wire without excessive insulation thickness.

Figure 6 shows how the primary of a low-power flyback transformer can benefit from these same techniques. Even in a small bobbin, it is possible to arrange windings in segments. In this example, about 22 turns are wound 1/3 of the way across the bobbin. We then have the choice of winding back on top of these windings, or using a turn to take the winding back to the beginning before adding another layer. This is knows as a z-wound segment, and it is used to minimize capacitance.

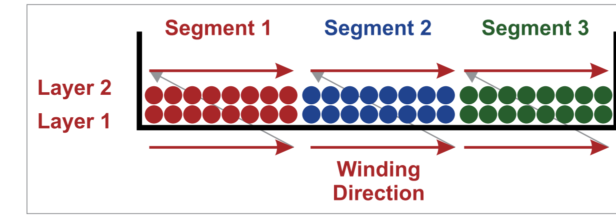


*Figure 6: Flyback Transformer Two-Layer Primary Z-Wound in Three Segments.*

This technique is repeated for three segments of the winding as shown in Figure 6. You can use this winding technique even if you are building a transformer by hand for prototypes. It is worth experimenting with this since the results are quite remarkable. Figure 7 shows impedance measurement of the segment-wound primary. The first resonant peak is now pushed out to 7.9 MHz, corresponding to an impressively low 6 pF of primary capacitance. This is more than a ten times reduction in primary capacitance, and it is achieved with no materials cost.

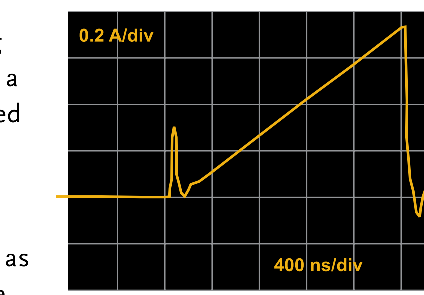


*Figure 8: Primary Switch Current with Minimum Capacitance Winding Layout. Notice the Greatly-Reduced Initial Spike and Complete Elimination of Ringing. Capacitance is Reduced to 6 pF.*

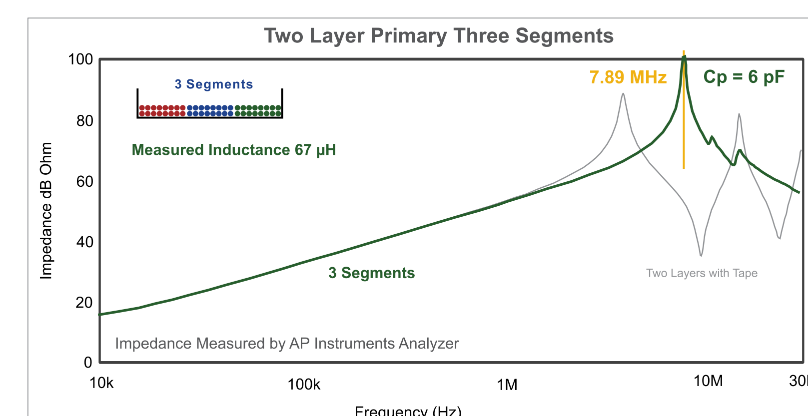


*Figure 7: Primary Impedance Measurement with Two Layers of Primary Z-Wound in Three Segments.*

You can also see form Figure 7 that there are no sharp resonant dips in the impedance. This has a direct impact on the circuit waveforms, as shown in Figure 8. The initial turn-on spike is reduced several times, and the current ringing is completely eliminated.

> The reduced turn-on spike greatly reduces the peak stress on the power FET, and reduces EMI. Without the following current ringing, it is much easier to tightly control the peak current without false tripping, and the converter can be much more ruggedly controlled.

**Summary**
Attention to the details of transformer windings can greatly improve the performance of your switching power supply. Simple changes to the high turns-count windings can greatly reduce winding self-capacitance. The improved winding techniques need not add significant cost to the design.

Even if you are working on low-power flyback converters, pay close attention to how the magnetics are wound, and do not be afraid to instruct your manufacturer to make changes to improve performance. You should also be willing to develop your own prototypes in the lab to test these concepts for your power supply.





# ISOLATED µMODULE POWER CONVERTER

## Improving Signal Measurement Accuracy

By Willie Chan

**Properly implemented, galvanic isolation is an effective defense against disturbances in the ground plane often referred to as ground loops, which occur as a result of varying electrical potentials.**

Physical limitations require that electrical components on a PCB connect to the ground plane at different physical locations. As a result, pockets of varying electrical potentials are created when each components' ground plane connection acts in combination with circuit board parasitics. Another significant contributor to the creation of ground loops is conducted EMI created by high current motors, pumps, switching regulators and digital processors with their characteristically fast changes in power demand often in the tens of amperes of current (Figure 1). These ground plane disturbances can result in significant measurement inaccuracies. The ground potential where the measurement sensor is located may not be the same as the ground potential where the ADC converted the analog signal to a digital signal. Thus the resulting digital signal is now skewed by the voltage delta between the two ground potentials. While compensation for the delta could theoretically be added at the signal processor, the magnitude of the ground potential delta changes over time as neighboring loads constantly vary their current consumption. This situation makes compensation a challenging proposition at best. Moreover, isolation offers protection for down-stream devices from potentially damaging supply rail transients or short circuit events.

**Galvanic Isolation Applications**
Dividing a large control system circuit design into smaller galvanically isolated compartments is a smart strategy to protect components the risks of damage from electrical overstress. The isolation barrier prevents any transfer of electrically charged particles therefore communication between compartments would be performed using other means such as optical, wireless, capacitive or magnetic methods. Any supply rail and/or ground disturbances can easily damage low power 5V or less sensor units comprised of ADCs, amplifiers, voltage references and transducers, which often have a combined power consumption below 1W depending on performance. As a precautionary measure, 500VAC (~710VDC) of galvanic isolation is inserted to protect these devices should a short cause the input supply voltage to exceed the components' absolute maximum voltage rating. In the event of such a failure, the resulting damage is limited to a small compartment or section of the overall control system. Additionally ground disturbances are also minimized which will be discussed in the next section. The damaged sub-sections may then be stocked or purchased as standard "off-the-shelf" replacement units enabling

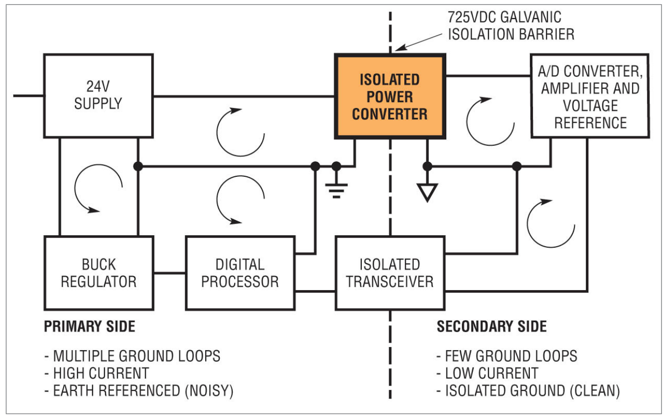


*Figure 1: Isolating power & ground rails for sensitive data converters, amplifiers & references from other high current power paths improves signal resolution & reliability*

a complete system recovery in a shorter amount of time with less effort.

**The Right Balance of Power**

Isolated power converters preserve signal accuracy by creating an electrical barrier between noisy high current and low current sections of the system where a cleaner more stable ground is available. In particular isolated DC/DC converters delivering under 2W provide sufficient power for one or more sensor units consisting of an amplifier, ADC converter, transducer and voltage reference (Figure 2). While isolated compartments consuming more than 2W may start to experience the same ground loop issues which called for galvanic isolation in the first place. Furthermore, as the isolated compartment increases in complexity, the additional wires and PCB traces inside become more susceptible to electrical noise generating sources such as radiated EMI from neighboring electronics. Given a stable ground plane protected by an isolation barrier, more accurate readings can be made by the sensor unit, improving system control. Accuracy may even be improved to the point of permitting system performance upgrades with higher resolution ADCs.

**Limitations of Conventional Isolated Converters**

Conventional power converters employed for 500VAC (~710VDC) isolation have a limited ability to support industrial and commercial applications. Many have a maximum internal operating temperature of +85°C. Including the effects of internal power losses and package thermal resistance, the output power of a conventional converter may start de-rating at an ambient temperature between +50°C to +65°C leaving little margin. Cooling systems can provide some assistance, however it raises other concerns in terms of cost, size and reliability should the fans fail. Other isolated solutions require a ±10% accurate 12V or 24V input which is incompatible with power from an unregulated power supply or an industrial Li-Ion battery whose usable voltage range varies by ±12% to ±14%. While conventional isolated converters offer common fixed output voltages such as 3.3V and 5V, they do not provide any flexibility to accommodate the 0.1V or greater dropout voltage of an external 3.3V or 5V reference nor a similar output voltage LDO post regulator. The latter may be implemented to reduce input power ripple for an A/D converter. As control systems become more complex, additional isolated sensor

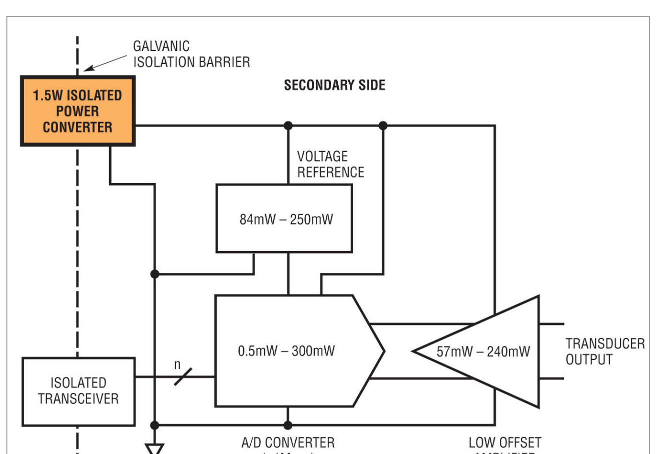


*Figure 2: Power Consumption range for each component in a sensor unit consisting of amplifier, ADC, transducer & Reference. Total power consumption is less than 1W.*

compartments are required to support a greater number of signal channels providing further information on system performance. At the same time board space is limited requiring a smaller solution size to fit more features into less space. A new advancement in isolated DC/DC power converters addresses these concerns.

Conventional Isolated Converter Limitations:

- Maximum Internal Operating Temperature of +85°C Limits Output Power
- in High Temperature Industrial Environments
- ±10% Input Supply Requirement Hampers Operation from Unregulated Power Supplies or Batteries with ±14% Voltage over Operating Life
- Internally Fixed Output Voltages do not Accommodate Dropout Voltage for 3.3V / 5V Output Voltage References nor LDO Post Regulators

**New 500VAC (~710VDC) Isolated Converters**

A solution which addresses these limitations is the LTM8048, a 725VDC isolated µModule® power converter. A space saving 1.5W output solution, the LTM8048 includes the power switch, controller, transformer, and compensation in a 9 x 11.25 x 4.92mm BGA package requiring few external components (Figure 3). The converter offers advancements in operating temperature, input and output voltage range compared to conventional isolated power solutions. Guaranteed to operate up to an internal temperature of +125°C, the 1.5W rated LTM8048 is better suited for operation in industrial and commercial applications such as natural resource delivery infrastructure, turbine, battery management, and security equipment. The wide input supply voltage from 3.1V to 32V allows the LTM8048 to be powered directly from less expensive unregulated switching power supplies or a wide range of battery stacks. Moreover, the primary side input voltage on the converter may be above, equal to, or below the desired output voltage on the secondary side. An internal LDO offers any output voltage from 1.2V to 12V adjustable simply by applying the appropriate resistor between the LTM8048's feedback pin and the secondary side ground. The output voltage features a ripple of less than 1mV providing a stable power rail for ADCs and analog sensors for more accurate and repeatable measurements. The internal 725VDC galvanic isolation barrier suitable for 500VAC (~710VDC) requirements is 100% production tested for guaranteed circuit protection.

**A Glimpse inside the LTM8048**

Within the LTM8048 is an isolated flyback controller, power switch, 725VDC isolated transformer, a modest amount of input and output capacitance, compensation and a low output ripple linear regulator supporting up to 1.5W of output power (Figure 4). The controller architecture and voltage feedback loop allows the LTM8048 to create an output voltage on the secondary side that is above, below or equal to the input voltage.

Some isolated controller ICs use opto-isolators or extra transformer windings to feedback voltage information. Opto-isolator circuits waste output power and the extra components increase the cost and physical size of the power supply. Moreover, Opto-isolators can also exhibit trouble due to limited dynamic response, nonlinearity, unit-to-unit variation and aging over life. Circuits employing extra transformer windings experience an increase to the transformer's physical size and cost, and dynamic response is often mediocre. In contrast, the LTM8048 control loop examines the switch voltage reflected to the primary side of the transformer to ascertain the secondary side voltage when the secondary side current is near zero. This novel approach to regulation enables the LTM8048 to support a wide range of secondary side output voltage which is selected simply by adding a resistor.

A switching cycle begins with the internal switch turning on. The inductor current increases until an internally set current limit is reached. The voltage across the power switch rises to the output voltage divided by the secondary-to-primary transformer turns ratio plus the input voltage. When the secondary current through the diode falls to zero, the voltage across the power switch pin voltage falls below VIN. A discontinuous conduction mode (DCM) comparator detects this event and turns the switch back on. Therefore, a smaller transformer can be used compared to an isolated converter, which always operates in continuous conduction mode.

An internal low output ripple linear regulator on the secondary side creates a low ripple power supply rail to support high accuracy A/D converters and low offset amplifiers. With the addition of an optional 0.01uF reference bypass capacitor the output voltage ripple decreases to less than 1mVp-p and 20μVRMS over a 10Hz to 100kHz range (Figure 5). Additionally, this reference bypass capacitor will improve the transient response of the regulator. Output voltage accuracy over the full temperature range is ±2.5%. The linear regulator is protected against reverse input and reverse output voltages.

Design innovations led to development of a compact 725VDC isolated transformer enabling a significant size advantage in the construction of the LTM8048 Isolated μModule Converter compared to other solutions. For added peace of mind, the module is 100% tested in production with

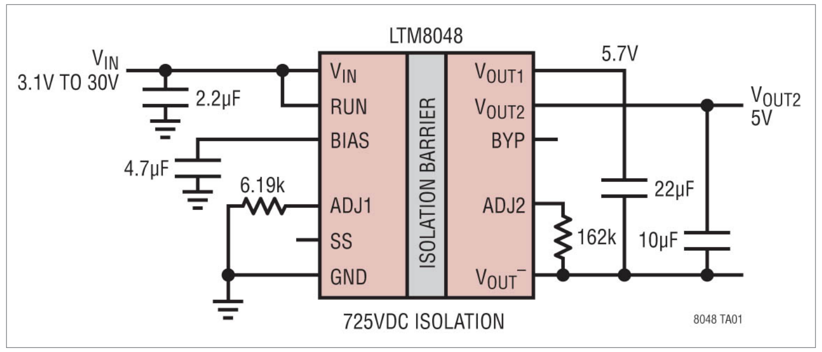


*Figure 3: LTM8048 typical application*

725V applied in both polarities for one second each.

To ensure consistent performance under the most demanding conditions, the LTM8048 is backed by rigorous reliability testing the results of which are posted online in an extensive report showing no failures to date. Reliability tests conducted include operating life, temperature cycling, thermal shock and board mount vibration to name a few. The LTM8048's BGA package is well suited for use in electronics targeted for high vibration environments. Furthermore, each LTM8048 converter endures extensive production testing at the extremes of the operating temperature range with particular care extended to the MP-grade rated for the -55°C to 125°C range (LTM8048MPY#PBF).

**Conclusion**

Isolated power is a proven method to protect and preserve the accuracy of low power sensor units comprised of ADC converters, references, amplifiers and transducers whose performance may otherwise be adversely affected. Correct and reliable data gathering by the sensor units is critical to control system operation. In most cases, the entire sensor unit consumes less than 1W using the latest components. Although conventional low power galvanically isolated DC/DC converters have provided a trustworthy and effective barrier they have shortcomings in the areas of input voltage range, output voltage range, maximum operating temperature and size. A new 1.5W μModule isolated converter broadens the application possibilities by offering advancements in input voltage range, output voltage range, and operating temperature in a compact surface mount solution. Moreover all μModule power products are backed by extensive reliability testing with the results available online. A more flexible and compact option is now available for design engineers seeking a 725VDC isolated DC/DC power solution.

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# CHALLENGE OF AUTOMOTIVE AUDIO

## Active Antenna Power Supply Design

By Kieran McDonald

In the age of connectivity, increasingly demanding consumer expectations are driving the evolution of in-vehicle infotainment, resulting in greater demands on the infotainment system power supply. In automotive audio systems in particular, the introduction of active antennae to enhance the power of the received radio signal, thereby improving the audio quality enjoyed by the consumer, demands an alternative approach to its power supply.

In the past, the radio antenna was typically composed of a passive receiving element with the signal being passed directly via cabling to the Audio Head Unit (AHU); in some cases this was located an appreciable distance from the antenna itself. The implication of this was signal loss, of an already possibly weak signal, and susceptibility to noise interference. An active antenna, however, makes use of an installed amplifier along with the passive receiving element, to amplify the received audio power, as well as providing a low noise and low distortion output, and an impedance matching function. The installed amplifier requires power and this is usually provided by the AHU, or infotainment system, as either an individual power supply cable or utilising the antenna High Frequency (HF) cable itself, the latter often being referred to as a 'Phantom Supply'.

The power supply could either be a regulated supply, a protected battery supply, or a 'raw' battery supply, depending upon the requirements of the active antenna amplifier IC. The challenge for the power supply is that there are a number of scenarios, either through faulty vehicle assembly or maintenance, which could result in the load becoming disconnected from the supply, shorted to ground or to battery. As a result the power supply needs some means of being able to detect the state of the load to allow the system to deduce whether it is operating within prescribed parameters or whether there is some fault condition present. Most vehicle manufacturers mandate this as a requirement, with the system distinguishing between fault types and displaying a fault diagnostic code on the audio display or the Multi-Function Display (MFD), as a means of assurance of correct assembly.

Current sense regulators, such as the ON Semiconductor NCV47700 and NCV47701, have been developed with these issues

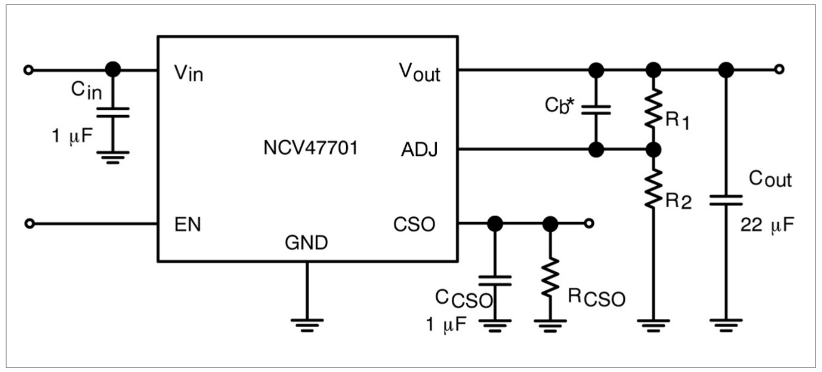


*Fig. 1 – The ON Semiconductor NCV47701 Current Sense Regulator Implementation*

in mind, measuring the current through the output of the device and providing a mirror current reference output, in addition to providing a linear regulated output voltage, with the input capable of being derived from the car battery.

**Introducing the Current Sense Regulator**

Current sense regulators make use of an integrated current mirror, providing the ability to diagnose fault conditions in the load. This is of particular importance in vehicle assembly where there is a risk that the AHU, the active antenna or the cabling between them may either be faulty or misassembled. As a result the risk exists that the current sense regulator output, VOUT, could be shorted to ground, left open or, to a lesser extent, shorted to battery. The current mirror provides a mirror current sourced through its output, the current sense output (CSO), which is at a fixed ratio (1:100 ± 10%) to the load current, which can be monitored as a voltage (VCSO) across a fixed resistor to ground, and can be sampled by an ADC for example. The resistor value, RCSO, also programmes the current limit threshold level. By monitoring the CSO voltage the current mirror can be used to distinguish between open circuit, short to ground and normal operating conditions.

In a short to ground condition the load impedance falls to zero, or near to zero, causing the load current to rise and tripping the externally programmed current limit, the output voltage folding back reciprocally. This causes VCSO to rise to its upper limit of 2.55V. Secondary protection is provided for with a second default current limit, set at an internal fixed value of 400 mA, with a faster loop response than the programmed current limit, guaranteeing current limitation at start-up. There is a further level of protection with a thermal limit threshold, detected by a Thermal Sensing Device (TSD), located next to the regulator linear pass element, to ensure that the 150°C maximum junction temperature, TJ (max.), is not exceeded. If the TSD threshold level is exceeded then the regulator disables itself until the threshold is crossed again.

In an open load condition the load current falls to zero or near to zero. Reciprocally VCSO falls close to ground potential with ICSO guaranteed to be no greater than 10 µA.

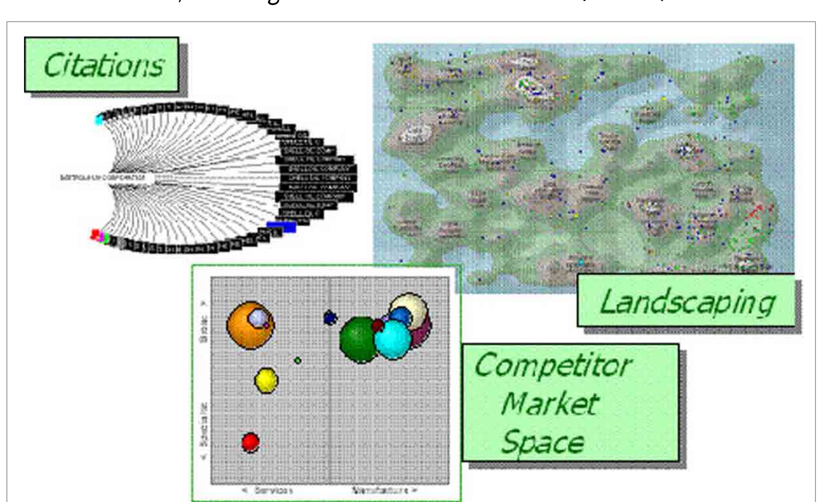


*Fig. 2 - The ON Semiconductor NCV47700/1 Current Sense Regulator Block Diagram*

## While a short to battery condition can't be directly diagnosed, using the VCSO output, the device is protected against conditions where VOUT is shorted to battery, either in a powered or an unpowered state.

**Current Sense Regulator Benefits**

The current sense linear regulator provides an alternative to discrete circuitry or high side switches, with substantial benefits. A typical discrete diagnosis and protection circuit might consist of over twenty discrete components and their ensuing assembly costs, and complex failure modes and effects analysis, as well as consuming valuable microcontroller resources for command and control purposes. The alternative current sense linear regulator is a single integrated circuit (IC), with only seven external small signal components. Additionally being an IC it has carefully controlled process parameters, such as current limit accuracy and current mirror ratio for example, which make the creation of a fault strategy, fault detection thresholds and worst case analysis, using the current sense output, straightforward.

The provision of accurate and adjustable output voltage regulation, including well defined limits of loop stability means that the fully protected output can be set to a target output voltage that correlates to the input requirement of the active antenna amplifier, with a loop that is stable with a low cost and standard equivalent series resistance (ESR) output capacitor. This compared to a high side switch output voltage which will not regulate but rise and fall in proportion to the input source - typically the car battery. The ON Semiconductor NCV47700/1, for example, has an adjustable output voltage, with the output voltage set by an external resistor divider, adjustable between 5.0 V and 20 V (NCV47700 has an output voltage tolerance of ±6% and the NCV477001 ±3%); the output is stable with a 22 µF standard ESR capacitor.

The flexibility, in terms of circuit programmability, inherent in a discrete circuit design can be achieved by the current sense regulator offering a programmable output voltage and current limit levels as well as an IC enable. The ON Semiconductor NCV47700/1 has an externally adjustable current limit, programmable between 10 mA and 350 mA by a resistor (RCSO) to ground, from the CSO pin. The current limit is accurate to ±10%, between 10 mA and 100 mA, and accurate to ±20%, between 100 mA and 350 mA.

**Conclusion**

Current sense regulators provide a simple integrated solution to power active antenna amplifiers, in automotive audio and infotainment applications. They provide the ability to monitor the status of the load, enabling fault diagnosis, and providing protection from fault conditions.

The ON Semiconductor NCV47700 and NCV47701 ICs are available in both SOIC-8 and SOIC-8 EP (exposed pad) packages. Designed specifically for use in the automotive environment, their input and enable pins can sustain an ISO-7637-2 load dump pulse (5b) of up to a 45 V peak.

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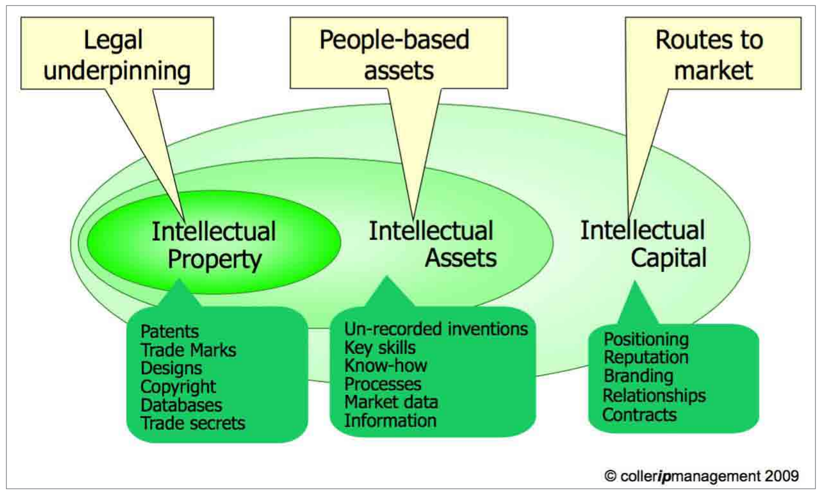
# POWERFUL IDEAS

## Protecting and commercializing the intellectual assets

By Jackie Maguire

An inventor caught up in the thrill of developing a new product, or an engineer trying to source parts from other companies to complete his new design, may understandably not have legal matters foremost in mind.

But unless lady luck is on his side, leaving the issue of intellectual property to some later date when he is less preoccupied could prove very expensive indeed. The big players in the electronics and engineering markets owe their success to a number of different factors. Being in the right-place at the right time, focussing on their core strengths and products, their ability to adapt quickly to change (especially in core markets), and a heavy involvement in setting standards are just some of them. Although much of their success could be attributed to their CEOs and other senior staff, it could not have been achieved without the talent and ingenuity of their engineers and designers. But at least as importantly as any of these factors, all these companies recognised and appreciated, right from the start, the value in continually creating core intangible assets that would be needed by them, their competitors and others. They saw intellectual property as an asset.




*How intellectual property, intellectual assets and intellectual capital work together*

Yet even large organisations do not always pay the continual attention to maximising their intangible assets that they should, and many one-person start-ups ignore it completely. It is vital that everyone involved in the company, from the CEO to the engineers, understands the value in protecting and commercializing the intellectual assets.

So what do we mean by the terms intellectual property, intellectual assets and intellectual capital? Most people assume that protecting their intellectual property means filing applications for patents or registering a trade mark, and that is certainly part of it. But the term intangible assets means far more than that. The various elements which make up an organisation's intangible assets are shown below.

Intangible assets do not consist just of patents and other formal intellectual property rights (formal IP) such as trademarks, designs and copyright – which are underpinned by various statutes and laws. Formal IP is only a piece of the intangible assets jigsaw. Intangible assets also include customer and business relationships, workforce skills, branding, business processes, reputation and the know-how of employees, including electronic engineers and designers. Ideas and inventions provide a company's heart beat, while the wider intellectual capital drives growth and future revenues.

Many small companies in the electronics industries have talented and inventive engineers yet the companies for whom they work fail – for a number of reasons - not only to protect, but also to commercialise, their designs and inventions which means they are not as successful as they could be. As a CEO or engineer in a start-up, you might think you are too small or specialised to be considered a threat by any of the giants with established IP. However, you should not forget that once the core product or process is marketed, unless IP protection is in place others may copy it, change it slightly and claim it as their own, leaving you behind with possibly potentially serious business consequences.

The risk of your core product, process or idea being stolen, or that your company is not the first mover you thought it was, can be minimised by understanding where you, as a CEO or engineer, can contribute to the intangible assets jigsaw and where the core products you are working on lie within the IP matrix. A question you should ask is; are you and those in your company willing to recognise and appreciate, ideally from the very beginning or as soon as possible, the value in continually creating core intangible assets that would be needed by you, your competitors and others?

At the very least, CEOs and engineers in the electronics industry need to be aware of what patents their competitors hold and how these may affect core products. You also need to be aware of the key elements of your core products. In this industry core products can range from a single component (e.g. A display, or chip), or several components working in unison to an entire product. And any of the components that make up your core product may be patentable or already patented by your competitors or suppliers which can be a risk for your business.

The electronics field is very crowded in terms of patents. Many small to medium sized companies in this area may not realise how vulnerable they are. Nowadays, a small company simply implementing a product that conforms to a standard can risk infringing another company's patent(s). A start-up company can inadvertently step on the toes of the "giants" due to a lack of understanding of the patent landscape within which the start-up is operating or is intending to operate. For some, this can end their aspirations to run a successful business.

Companies of all sizes should take advice on their freedom to operate in relation to their core product(s) and also on how they can establish their intangible assets - for example, when should they patent their inventions? And how should they go about it? To build a patent portfolio that is worth cross-licensing, there needs to be patents and/or good pending patent applications in it.

So what is a "good" patent or patent application? As a patent defines an invention, it is the scope of this definition of the invention that can prevent others from making it. At the very least, a "good" patent should: 1) have a broad definition of the invention; 2) cover obvious work-a-rounds or variants; 3) still be commercially applicable to the business; 4) cover the aspects of the core product that implements the invention.
In order to obtain a patent, an invention should be novel (that is, the essence of the invention has not been made available to the public in any form before the filing date of the patent application) and inventive (i.e. not obvious over all mankind's knowledge so far).

An invention is obvious if a person skilled in the art (that is, an "unimaginative" expert in the field - this is a fictitious person), whom using their common general knowledge and the documents available to them prior to the filing date of the patent application, i.e. the invention, would have found it obvious to modify or adapt these documents or knowledge to put the invention into effect.

Formal IP law can be complex, but to ensure that your particular trade mark, design or invention is properly protected, in all the relevant jurisdictions/markets – organisations sometimes think they are fully protected internationally when in fact they are not - the advice of a specialist intellectual property lawyer or patent attorney can make good business sense. It is important to find a lawyer or patent attorney who is within your budget, has an excellent technical grounding in electronic engineering, computer science, and/or physics, who is not only able to understand a complex technical brief quickly, can draft a specification rapidly, but also is able to engage with engineers and the inventors and draw out alternative embodiments or examples of the invention, and alternative ways of doing something, in order to fully claim the invention.

Protecting intangible assets is vital. But that is only part of the process. It is important not just to protect but also to understand the commercial value of the intellectual assets and ensure that you are fully exploiting them, having a clear idea of the commercial goal from the outset.

*Lithium-ion patent landscape*

Choice of business model is the key to considering whether value is realised from manufacturing, production, direct sales or licensing. For some companies with the correct experience and know-how it makes sense to manufacture a new product. For others, a license to an established manufacturer/supplier is the best way to get a return from your invention. The correct business model, product proposition and route to market need to be laid out as inputs to an IP strategy ideally from the outset, so that the best form and details of protection can be established. In addition, market issues need to be factored into the process to guide and inform the key IP decision making steps along the way. Some companies – including Coller IP – use sophisticated landscaping tools to help 'map' competitors.

Despite the market downturn, new opportunities to trade internationally are still being created and there are real opportunities for companies who can provide products or services that will be taken up by the marketplace and to make money from their intangible assets. However, companies need to ensure that, in taking advantage of these new opportunities, they do not leave themselves open to exploitation, that they understand value of the 'hidden treasure' they hold and how to maximise its potential going forward.

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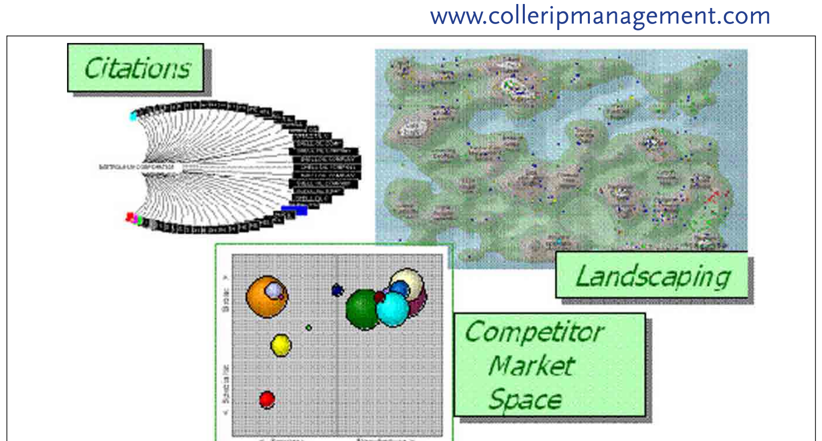


*Examples of outputs from analytical tools*



# Special Report: Renewable Energy

PSD NORTH AMERICA
Power Systems Design: Empowering Global Innovation

## Inside:

# DIGITAL POWER

## For Higher Efficiency

By Laurence McGarry and Ken Marasco

Compared to traditional analog PWM controllers, Digital power controllers provide an extremely high level of flexibility and programmability over the serial interface bus.

The designer now has the capability to optimise performance by making changes in software, adjusting the parametric performance of ICs and affecting the functionality of the system. Some examples could include margin and position the output voltage to optimise load performance, changing start-up and shutdown timing to ensure reliable system turn-on and off, altering the control loop compensation to optimise bandwidth and transient response, and fine tuning the timing delays to optimise efficiency.

As the system is integrated, it now becomes possible for system architects to make dynamic changes based on the system load behaviour. Some examples could include: dynamic changes of the control loop at different temperatures or load different load conditions; and, dynamic changes to improve the efficiency of the system – changing voltage,

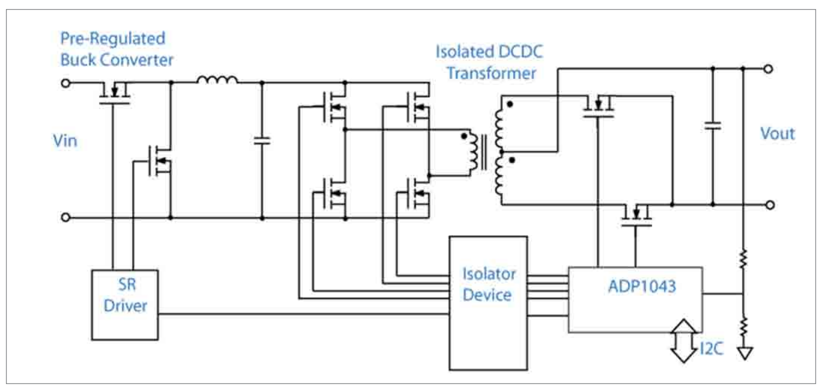


*Figure 1: Two-stage DCDC with pre-regulated buck converteer with DC transformer islolated stage*

delay timing, switching frequency and phase shedding at light load conditions in multi-phase applications.

Enabling Energy Efficiency
The energy efficiency of a power converter is largely dictated by the topology and then the power silicon, copper PCB and wire and interconnects in the high current path. However, there are some subtle ways that digital power can be used to improve energy efficiency.

With reference to Figure 1, here we introduce a two stage DCDC topology, where the input voltage is converted down to a lower fixed voltage, the second isolated stage now runs as an open loop DC transformer with high duty cycle. While the first stage does incur losses, it does regulate changes in the input and allows the second stage to operate at very high efficiency. Results depend on the application and power level but typically around 1% efficiency improvement is achievable in high power ACDC applications.

This energy efficient topology is not necessarily new. However, as shown this is controlled by a

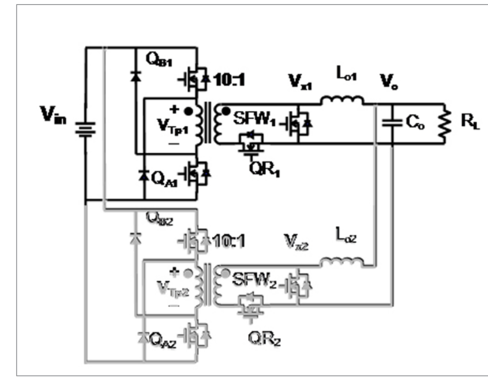


*Figure 2a: Interleaved forward converter can be controlled by digital controllers with ability to disable phases at light load for reduced losses*

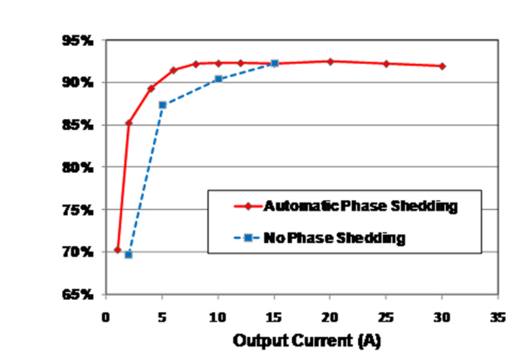


*Figure 2b: Measurement results for a 300w interleaved forward. Light load efficiency can be improved by around 15% by disabling the phase*

single digital control and monitor IC, ADP1043A, with few required external components. While the topology is driving the efficiency improvement, it is being enabled, or made possible, in a cost effective way by the use of the digital controller.

Many end applications never operate at the maximum designed power level. For example, servers typically operate at around 20-30% load. Consequently, it is essential that the power converter operates efficiently across the entire load range of the application. Figure 2a shows an interleaved (two phase) forward converter with synchronous rectification which can be controlled by a digital controller, such as ADP1043A. The converter operates both phases at high load operation but sheds a phase at lighter loads, where it is more likely to operate during the product life cycle. By taking the components out of the power path and by reducing the switching transitions on one half of the converter, significant savings in efficiency can be demonstrated at lower loads as shown in Figure 2b for a 300W converter. Again, this topology is not a new concept but the implementation and the efficiency improvement are enabled by the digital controller, ADP1043A. The digital controller can enable flexible and smooth transitions between states. Further efficiency improvement at low load can be made by utilising the adaptability of the digital controller and finely adjusting the gate drive timing delays between drives. Again, this will help to improve the efficiency over the entire load range.

In ACDC systems, system designers add power factor correction (PFC) to meet mandatory power factor and harmonic distortion requirements but also to improve the overall system efficiency. Low power factor increases the peak current and can increase system losses. The use of digital controllers to perform the PFC function and to provide accurate input power measurement has become more popular due to the flexibility and the performance improvements achievable. Analog Devices has recently introduced the ADP1047 single phase, digital PFC with accurate power meter followed by the interleaved version, ADP1048, for higher power, compact systems. Both devices enable efficiency improvements at light load by providing programmability over the frequency and the PFC output bulk voltage. An outline schematic of the ADP1047 is shown in Figure 3 with an indication of some of the key features.

**Improving Efficiency through Intelligent Power System Management**

The ability to read parametric and performance data via the serial interface and dynamically adjust functionality, allows the system architect to implement an intelligent power system to improve the overall system efficiency. A server operating at, say, 20% of its specified load may be supplied by a number (typically 2 or 4) of parallel ACDC power supplies providing N+1 redundancy with forced current sharing to ensure that workload

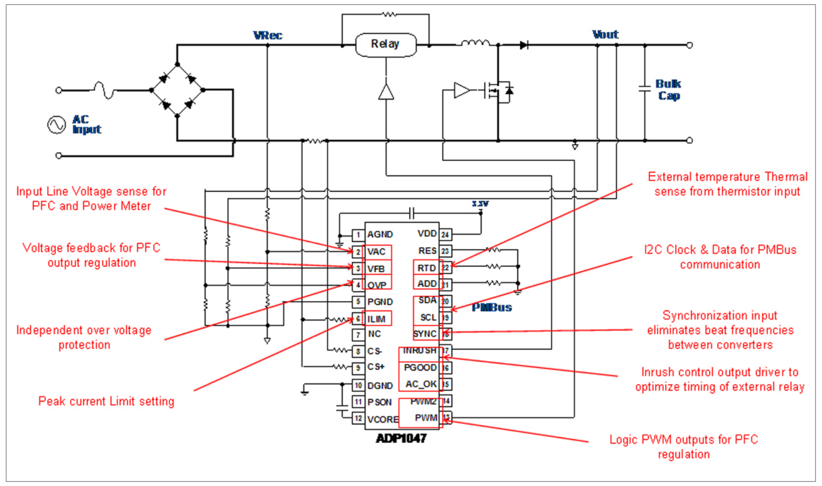


*Figure 3: ADP1047 - Digital PFC with Accurate AC Power Meter in Single Phase Application*

and heat are spread evenly. In this condition, the ACDC supplies are operating well below their optimum operating efficiency. With knowledge of the system load, the system architect can now configure 2 of the 4 ACDC supplies to a high efficiency standby mode while the other 2 now operate at a higher loading closer to their optimum designed efficiency. The net effect is that the overall system efficiency improves without compromising the reliability or uptime. Similarly this concept could be applied to telecom -48V DC input systems that have parallel, input modules current sharing.

This concept is being extended to higher level system implementations; workload or power consumption can be accurately measured and communicated to a master controller or system manager allowing workload to be redistributed between system blades or line cards, or between server farms or data centers. Workload can be 'virtualised' to improve overall network efficiency and possibly even to improve redundancy and availability of capacity.

Intelligent Power Management can be extended to provide a number of other system benefits including: the ability to accurately measure

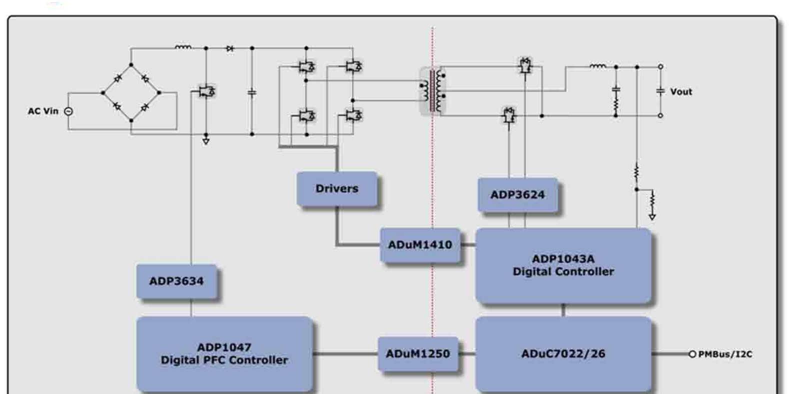


*Figure 4: intelligent Power Management system to enable energy efficiency through flexible., digital controllers*

power allows the system architect to apply only the necessary amount of cooling required, thus reducing the power consumption of the thermal cooling system; data recording via the serial interface could store valuable historical performance data to a next generation designer or an engineer analysing failure returns – effectively a power system 'Black box flight recorder'; predictive failure capability that flags a system component that must be replaced at next service; and increased resolution for remote diagnosis of failures. The two latter points reduce service time on site and could significantly reduce maintenance costs.

Figure 4 shows one implementation of such an intelligent power management solution. In this case, the ADP1047 digital power factor correction controller with accurate power metering controls the conversion from AC to bulk DC. The isolated DCDC is controlled by the ADP1043A digital controller located on the secondary side of the isolation boundary. Both controllers are capable of communicating parametric and performance data. Dependent on the complexity of the data gathering required, an additional micro-controller can be added on the secondary side to communicate with the PFC device and the DCDC controller. ADI iCoupler isolation technology enables high speed communication across the safety boundary.

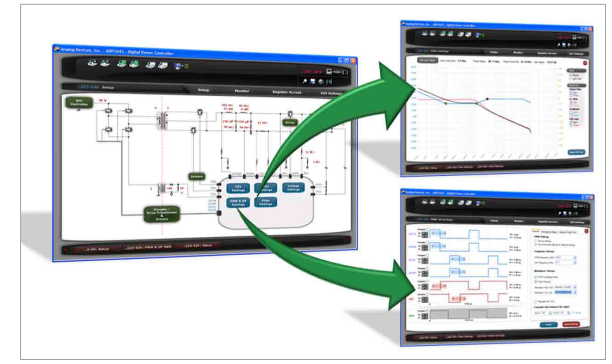

*Figure 5: Programming via intuitive, easy to use Graphic User Interface. No programming skills required. Figures show that the loop bandwidth can be manipulated to optimize transient response and the PWM timing optimized for efficiency Improvement*

**Practical Implementations in Digital Power:**

Some examples of the new breed of digital power devices are ADI's ADP1043A digital PWM (pulse-width modulation) power control and the ADP1047/48 digital PFC with accurate power metering. These new devices provide designers with highly integrated circuit architecture and the flexibility to configure system power-supply parameters in a matter of minutes using an intuitive GUI. Power design engineers with no prior programming experience can use the GUI to monitor and quickly adjust power functions such as frequency, timing, voltage settings and protection limits.

Figure 5 presents some screen shots of the easy-to-use, windows based GUI. The user enters GUI with the familiar schematic of a power supply and can then choose which feature should be adjusted. For example, the bandwidth of the power supply is modified by changing the position of the poles, zeros and system gain. The switching converter topology can be selected and the timing adjusted for optimum performance.

All the changes are made easily from the engineers' computer – changes can be made dynamically while the system is operational. In effect, the designer can observe real-time the impact of changes being made.

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# EFFICIENT UTILIZATION

## Three-Phase Power

By Neil Symonds, and Patrick O'Shaughnessy

As a designer and manufacturer of critical power systems used in airborne, shipboard and ground-based applications in the defense and commercial markets, Excelitas Technologies recognizes the need to optimize overall system efficiency.

The conversion of three-phase power to a DC voltage using a bridge rectifier results in the generation of large line harmonic currents. These result in excess losses in the power distribution network, which is designed to distribute current at the fundamental frequency of the supply, not at high order harmonic frequencies. Harmonic currents also cause harmonic distortion of the voltage waveform of the supply, which adversely affects the performance of rotating machines connected to the same supply, and can cause them to draw more current than they should. For these reasons, it is desirable to convert three-phase to DC voltage in a manner that does not generate significant harmonic currents in the supply. There are also regulatory requirements in some environments. For instance, commercial aircraft power utilization equipment must meet the requirements of RTCA/DO-160, which sets strict limits on the various line harmonic currents as a percentage of the fundamental current. On board Navy ships, MIL-STD-1399 Section 300 specifies a 3% limit for line harmonics. Excelitas offers two solutions to this problem, both of which are applicable to 60 Hz supplies and 400 Hz power systems.

The use of a multi-phase transformer-rectifier unit (TRU) has been well known for several decades. In these TRUs, the secondary winding is tapped and "wings" coupled to other phases are connected to produce six, nine or twelve output phases. These phases are rectified by a bridge rectifier with twelve, eighteen or twenty-four rectifiers to produce the DC output current. The line input current becomes a stepped waveform resembling a sine wave; the more steps, the closer it resembles a sine wave, hence the lower the harmonic content. In theory, for a TRU with N phases, all harmonics up to 2N-1 should be eliminated, and the amplitude of the first harmonic should be approximately 1/(2N-1). Excelitas Technologies developed its first TRU twenty-five years ago for a Navy program, which it determined could be met with a fifteen-phase unit, and was subsequently granted a patent for it.1 The fifteen-phase design offers superior performance over designs with fewer phases, but requires close attention to the accuracy of the phase amplitudes and angles, as this directly affects performance. Excelitas has developed techniques to ensure a high degree of control over these parameters. Figure 1 shows the harmonic performance of a TRU in a 400 Hz commercial aircraft system. The amplitudes of the harmonics are shown as blue bars, and the DO-160 limits are shown as red lines. As expected, all harmonics are below the limit up to the 29th; at this frequency, 11.6 kHz, the remaining harmonics are easily removed by a simple EMI filter.

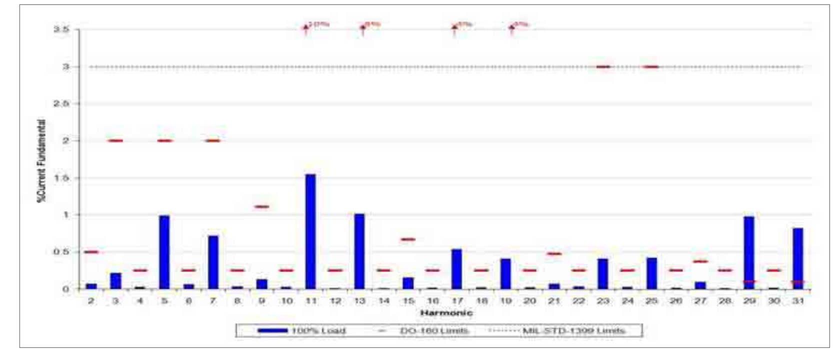


*Figure 1: Harmonic Performance*

Since the introduction of its first TRU, Excelitas Technologies has developed numerous units for 60 Hz and 400 Hz applications, ranging from 750 watts to 25,000 watts. Excelitas also offers autotransformer versions, which are particularly useful in reducing weight in airborne applications. TRUs are often used in high power motor controller applications in aircraft, where electric motors are displacing traditional hydraulic systems for moving the control surfaces of the aircraft. The high thermal mass of the TRU allows these units to be safely overloaded by a factor of three or four for the duration it takes to move the position of the flaps or other control surfaces. Figure 2 and Figure 3 show two examples of modern TRUs. As a rule of thumb, 400 Hz ATRUs weigh approximately 3 pounds per kilowatt, and 60 Hz TRUs weigh about 15 pounds per kilowatt. The variation is due to the extra iron for the magnetic circuit required in a 60 Hz transformer, as compared to a 400 Hz transformer.


*Figure 2: 1200 Watt Airborne ATRU*

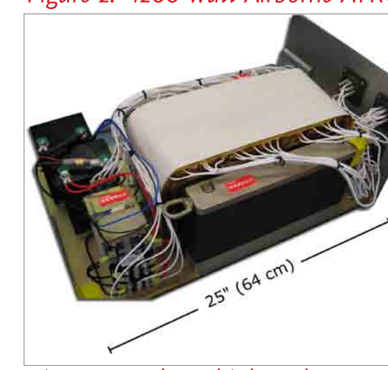


*Figure 3: 15 kW Shipboard TRU*

While the TRU is a simple and reliable solution to line current harmonic reduction, some applications require a solution that is smaller and lighter. For these situations, a class of all-electronic converters is available using high-frequency switching, which allows the magnetic components to be shrunk dramatically in size and weight. The schematic of the power train of one such solution is shown in Figure 4. This is akin to three boost converters, such as those used in single-phase power correction circuits. When a bidirectional power switch is turned on, the right-hand end of its inductor is connected to a point that mirrors the neutral point, although the neutral of the power source is not connected, and the magnitude of the current in the inductor increases with its polarity being the same as the instantaneous polarity of the source voltage. When the power switch is turned off, the polarity of the voltage across the inductor reverses and increases in magnitude until one of the rectifier diodes is forward biased and energy is discharged into the output capacitors, C10 and C11, and the load. The input current can be shaped to be sinusoidal by judicious control of the power switch duty ratio. The high-frequency component of the inductor current is removed by and EMI filter (not shown in Figure 4).

Excelitas Technologies has developed a 5 kW unit using this principal, switching at 400 kHz, and has now moved on to develop a second generation model in which the power switches are connected in a delta configuration, thereby eliminating the artificial center point. The advantages are better utilization of available state-of-the-art semiconductor devices, and improved independent control of the three phase

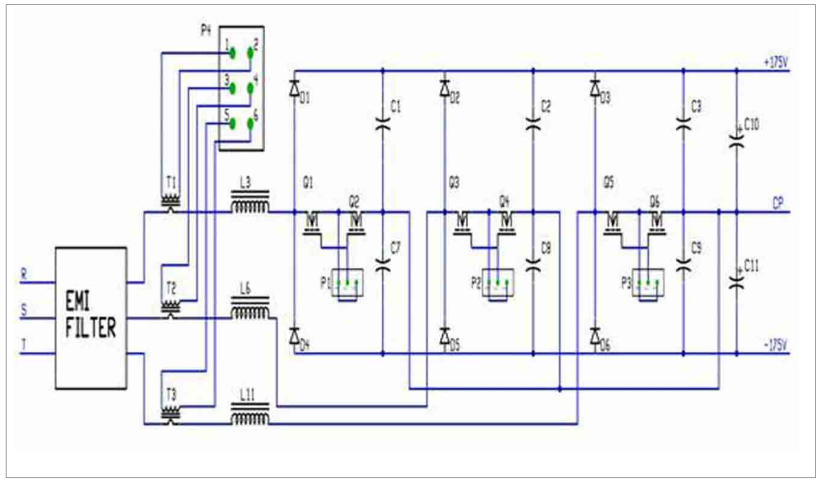


*Figure 4: Power Train Schematic Diagram*

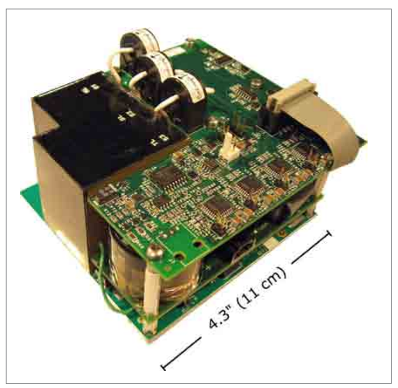


*Figure 5: 5 kW Power Factor Corrector*

currents, resulting in improved harmonic performance. This configuration is expected to outperform the traditional TRU in terms of harmonic reduction. The 5 kW converter is shown in Figure 5. Because the magnetic components are switched at high frequency, 350 kHz in this case, the same converter can be used in either 400 Hz or 60 Hz applications with only minor changes. The second generation is being developed for wild frequency aircraft applications, where the line frequency can range between 360 Hz and 800 Hz. The converter, not including its EMI filter, occupies 26 cubic inches for a power density of 192 watts per cubic inch. The weight is 1.95 lbs, equivalent to 0.39 pounds per kilowatt. Multiple converters can be connected in parallel with the aid of a simple load sharing circuit, to obtain higher output powers.

The all-electronic solution has already demonstrated performance and efficiency equivalent to the traditional TRU, and is cost-competitive at the 5 kW level. Moving to a digital implementation of the control electronics will greatly reduce the number of parts in the unit, leading to better predicted reliability. In this respect, multiple units in parallel can be used in N+1 redundant configurations, which leads to greatly improved apparent failure rates.

## Excelitas continues to design and manufacture TRUs and ATRUs for a variety of airborne, shipboard, and ground-based applications. The customer base is comfortable with the simplicity of the solution and its proven reliability. However, Excelitas believes that ultimately the all-electronic solution will displace the traditional TRU as its advantages become apparent and its reliability is proven.

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www.excelitas.com/ProductPages/Power_Supplies_-_Defense_Products.aspx





# INNOVATIVE DRIVES

## Product family for consumer and low cost industrial inverters for drive applications

By Wolfgang Frank

The megatrends in consumer drive systems are unbroken: The numbers of units are growing and so are the number of comfort features and quality requirements for the drive.

With Infineon's SOI technology the integrated circuits on the top side of the IC are separated from the deep substrate by a buried silicon oxide layer. The buried silicon oxide provides an insulation barrier between the active layer and silicon substrate and hence reduces the parasitic capacitance tremendously.

Moreover, this insulation barrier disables any kind of leakage or latch-up currents between adjacent devices. This results in an extremely high robustness against any kind of negatively biased nodes which are connected to the IC. As an example, the motor phase node is allowed to dive below the VSS potential down to -50 V for duration of 500 ns, which is the largest rectangular negative transient SOA of monolithic gate driver IC worldwide. The available devices are high-voltage and low-voltage MOS transistors, different diodes and passive elements like capacitors and resistors of various values.

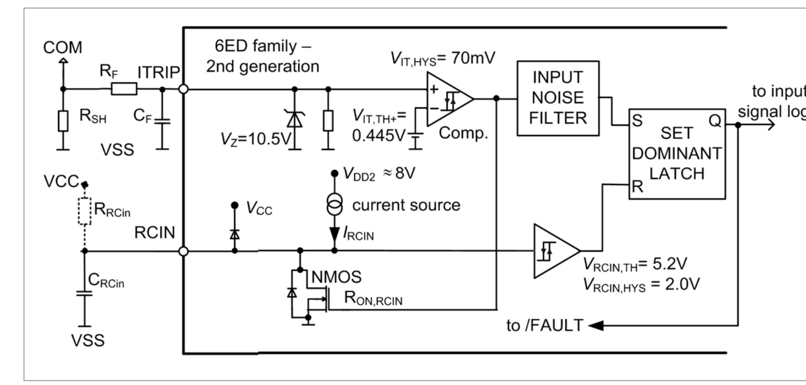


*Figure 1: Internal structure of the ITRIP and RCIN sections*

**Special feature set**

The 6ED family – 2nd generation contains various comparators which are helpful in the application in order to avoid external circuits of external comparators and their biasing circuits. This section describes the individual functions and features.

**Safety relevant shut down options**

The 6ED family – 2nd generation offers a couple of independent options for a shutdown of the inverter. First of all, the enable comparator can be used. The signal applied to pin EN controls directly the output sections. All outputs are set to LOW, if the signal is lower than VEN- = 1.3V typically and operation is enabled with signal levels higher than typical VEN+ = 2.1 V. The internal structure of the IC contains a Schmitt-Trigger. The typical propagation delay time from EN to the output sections is here tEN = 780 ns.

The IC is steadily enabled,

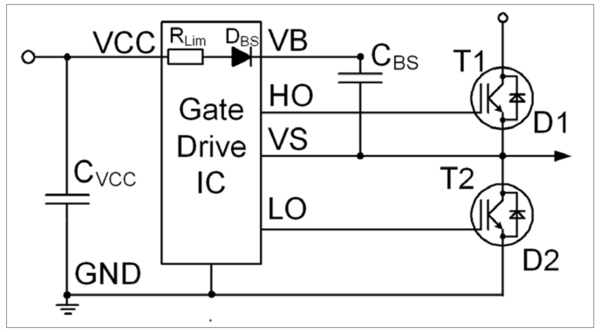


*Figure 2: Bootstrapping with 6ED family – 2nd generation*

when the EN pin is pulled up to VDD (i.e. +5V / +3.3V). It is not recommended at all to pull this pin up to VCC, because this may lead to excessive power dissipation in the input structure of this pin and could destroy the IC.

The second and most striking feature is the comparator at pin ITRIP. The comparator's threshold is designed to be directly connected to a low inductance shunt resistor RSH by means of an RC filter (RF, CF) according to Fig.1.
The output of the comparator passes a noise filter, which inhibits an over current shutdown caused by parasitic voltage spikes. The typical filter time of the noise filter is tITRIPMIN = 210 ns. A set-dominant latch stores the over current event until it is reset by the signal provided from the RCIN circuit.

The ITRIP-comparator activates also the discharging NMOS-FET at pin RCIN. The RDS(on) of the FET is typically 40 Ω, so that there is a characteristic discharge curve in respect of the external capacitor CRCin. The time constant is defined by the external capacitor CRCin and the RDS(on) of the FET. The discharge phase ends, when the comparator output at pin ITRIP is low again. This corresponds to a voltage level at the comparator of VIT,TH+ - VIT,HYS = 445 mV - 70 mV = 375 mV, where VIT,HYS = 70 mV is the hysteresis of the ITRIP-comparator.

The failure status is latched for a user programmable time, which is the charging time constant of the external capacitance CRCin and the internal current source. The source provides the current IRCin. Thanks to the current source an additional external charging resistor is not required. The /FAULT signal is activated while the failure status is latched.

**Integrated bootstrap diodes**
The integration of bootstrap diodes into 6EDL04I06NT, 6EDL04I06PT, 6EDL04N06PT and 6EDL04N06PR is the most striking achievement of the new generation of 6 channel gate driver IC. Bootstrapping is the common way to supply floating high side sections and was done by means of 600 V ultra fast switching diodes and a current limiting resistor in series. The ultra fast switching diodes are the simplest way to have a charging current to CBS, when the node VS is virtually GND, i.e. when the low side IGBT T2 is turned on according to Fig.2. Using the 6ED family– 2nd generation saves therefore up to three resistors and three ultra fast 600V diodes.

Large forward resistance values can lead to large voltage variations on the bootstrap capacitor as a result of sinusoidal pulse width modulations (PWM). It can be shown analytically, that this can even lead to temporary under voltage lockout situations, which must be overcome by large bootstrap capacitor values. The 6ED family – 2nd generation now offers much smaller forward resistance, which helps to keep the bootstrap capacitor small and cheap. Furthermore, the 6ED family specifies also a maximum value of 60 Ω, where none of the market competitors do. Furthermore, bipolar structures such as diodes are more robust against temperature increase in terms of forward characteristic. That means that the use of a real bootstrap diode widens the area of operation, whereas the use of integrated FET structures reduces the area of operation even more.

**Negative Transients at High Side Reference (pin VSx)**
The 6ED family – 2nd generation is very robust against negative transient voltages thanks to the inherent oxide insulation of the SOI-technology. Such transients may occur due to stray inductances in the physical setup.

Parasitic inductances can induce voltages vind(t) , which have an amplitude of the duration T so that the potential at pins VS1, VS2 or VS3 becomes negative in respect to pin VSS. It is a well known failure mechanism of other driver IC technologies that these negative voltages force current through the substrate material. The substrate currents can lead to a latch of the high side gate driver, which is then insensitive to any control signal for several milliseconds. The result is, that the IGBT are operated in repetitive short circuit, which leads to excessive power dissipation and finally also to system breakdown.

Therefore, the minimum voltage at the pins VSx is specified to -50 V for a period of time of 500 ns. This duration is long enough to cover the usual requirement for this stress in drives applications. Usual switching transitions are finished inside this window.

However, it must be the target of any design to avoid such negative voltages at all.

The negative voltage can also increase the pulse current through the external or internal bootstrap diode and may lead to damage. The design target is therefore to avoid such negative transient voltage at all or to keep at least the absolute maximum ratings.

Output current characteristics
The output current characteristic shows typical sink currents of 380 mA and source currents of 170 mA. The test condition gives a helpful condition for design engineers. The switching transition of power transistors takes place, when the gate voltage reaches the miller voltage according to Fig.3. The miller voltage is approximately between 5V – 7V. It is important to have a sufficient gate current capability in this area in order to avoid being too long in the linear region of power transistors and to reduce switching losses. It is therefore especially the current capability in the miller region, which is important for the application. The test condition of the 6ED family – 2nd generation is specified to the average output current in a window between 20% and 40% of the gate voltage amplitude according. One can see that this covers well the area of the miller voltage and the application can be nicely fine tuned.

It is easy to understand, that other output current specification such as a short circuit condition, is not appropriate here to fine tune the application. However, characterization measurements show, that the 6ED family – 2nd generation also provides competitive values for the short circuit test condition

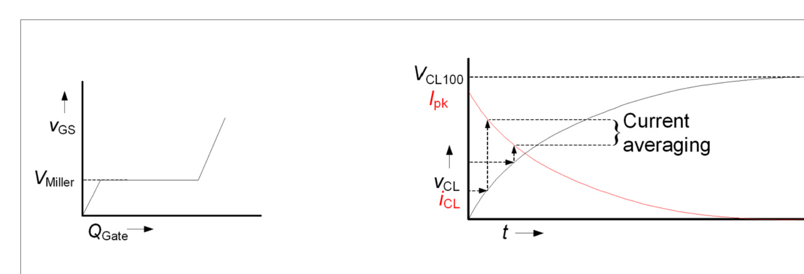


*Figure 1: Internal structure of the ITRIP and RCIN sections*

**Conclusion**
The 6ED family – 2nd generation is an innovative and intelligent driver IC. Its various options for shutting down the inverter offer a lot of opportunities to fine tune the application. The integrated bootstrap diodes can save external components on the system side. The gate drive outputs are powerful enough for all consumer drive applications and home appliances.

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www.infineon.com

# ENERGY SAVINGS

## Using closed loop voltage scaling control

By Randy Skinner

Wouldn't it be nice to save 25% to 30%, or even more, in circuit board power dissipation in your next design?

While for some designs such a savings would just be nice to have, for others it's a necessity to make the design competitive using the latest high performance integrated circuits. Why? Because the new ASICs, SoCs and processor technologies can be described in only one way –they are HOT!

What led to this problem? The answer is increasing power density in IC technology. Even with shrinking transistor sizes and lower operational voltages, the number of transistors on a chip, and the frequency at which they switch, has increased at an even greater rate. The result is more power dissipated in a smaller area that ever before.

**Converged Network Adapter Evolution**

In the converged network adaptor market, integrated ASICs combine the functionality of a network interface card (NIC) with an Ethernet processing core and a host bus adapter (HBA) using Fiber Channel processing cores.

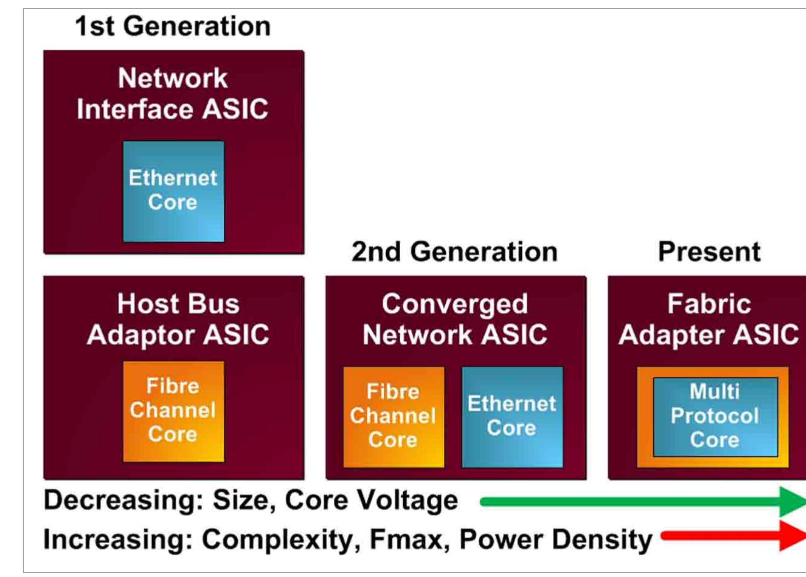


*Figure 1: Development of Converged Network Adapter ASICs*

Figure 1 traces the development of these highly adapted ASICs from separate functional ICs to devices with multiple core types on a single system on chip (SoC), to the present day Fabric Adapter ASIC capable of handling multiple protocols natively via a single IC core. This feat is accomplished with smaller process nodes and higher transistor counts than ever before possible. Multiple and lower operating voltages, along with higher clock switching speeds, facilitate this processing power in a smaller footprint than previously possible.

While this advancement is exciting, there are limits to any technology, including these powerful new ASICs. Board designers who use these technology-enabling ICs now have more challenges than ever to deal with. In small, compact board area environments, the design challenges created by higher power densities include:

- High local IC temperatures, which are near or at specified maximums
- The need for heat sinks or use of other heat mitigation measures
- Increased operating temperatures of adjacent devices

**Power Management Strategy via Voltage Supply Scaling**

Using the example of the converged network adapter card, a new technique for lowering power dissipation is to lower the core operating voltage(s) of the ASIC in question. This is done while making sure manufacturer-specified operating conditions are maintained. The savings can be significant, as the power dissipated is a function primarily of the square of the operating voltage of the device. When load and digital processing conditions permit, the Vcore of the advanced ASIC can be reduced with power savings of 30% or more per IC. Those conditions include I/O loading, clock speed and other parameters such as temperature and operational characteristics.

At appropriate times a circuit designed to control the setting of the Vcore of the ASIC can change the Vout of the supply delivering that voltage. In Figure 2 a dedicated MCU communicates with the ASIC and by implementing a closed-loop trimming algorithm adjusts the Vcore DC-DC converter in real time. The MCU measures Vcore from the DC-DC and then sends digital correction signals to the DC-DC via a voltage generated with an external digital-to-analog converter (DAC).

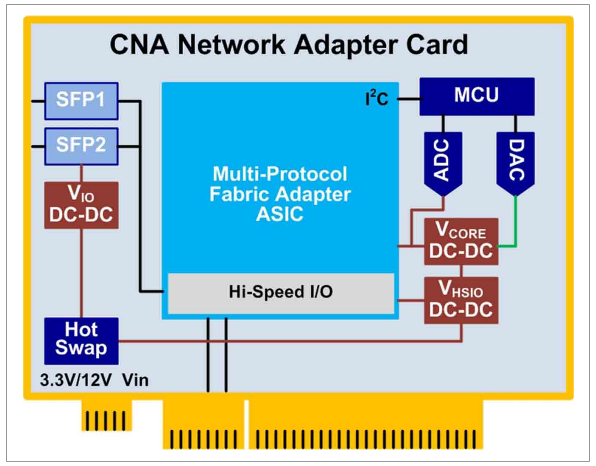


*Figure 2: Converged Network Adapter Voltage Scaling Solution*

**Challenges of Traditional Voltage Scaling Methods**

One of the challenges of implementing a working solution for setting the Vcore power supply to multiple values is the need for multiple external components in a closed loop control configuration. The measurement of the power supply output voltage is subject to the accumulation of errors created by ground potential variations and single-end voltage measurement techniques. Another disadvantage of single-end measurement is that it is not immune to noise. Traditional single end measurement is a poor alternative to differential input sensing and results in accuracies no better than 1.5% error (min). Other MCU-based solution challenges include the need for an external watchdog timer to insure that a hung processor condition does not occur. Finally, a custom-built solution is the most expensive alternative, especially when a large number of discrete ICs are required. Another item often overlooked is the risk and complexity of the stable closed loop trimming algorithm itself. A hung MCU or over-ranged ADC or DAC condition will result in unpredictable operation. Being too conservative and missing specification values will reduce power savings.

**A Complete Power Management Solution**

In addition to accurately scaling Vcore for multiple operating values, a complete board management solution should offer all of the following features:

- Voltage monitoring (all supplies)
- Power supply sequencing
- PCIe requirements for hot swap of 3.3V and 12V
- Power feed control to SFPs
- Reset Tree generation
- I2C link for multiple purpose communications

**Power Management Integration Benefits**

When there is an opportunity to scale supply voltages in applications such as the advanced CNA ASICs, it is important that the programmed voltages be adjusted automatically with speed and precision. To take advantage of lower operation voltages, the adjustment must also be stable over time, temperature and process variations. Using an integrated single chip solution such as the Lattice Platform Manager to set multiple Vcore values insures less than 10mV max error in Vout values over all the conditions noted above. Due to its programmability and simulation capabilities, the Platform Manager device is easy to implement and verify precision operation. Differential sensing is incorporated on these platform management products as a standard feature that makes them immune to errors due to ground voltage difference.

A key benefit derived from setting the DC-DC to a very precise value is that maximum power savings are enjoyed without violating the manufacturer's minimum setting and endangering reliable device operation. In other words, if operation at a lower power setting is allowed, it is important to take advantage of it, since the clock rate will be also be lowered. Any operating voltage higher that the precise minimum allowed would fail to achieve maximum savings while also forfeiting precious performance margins. Precise, closed loop setting of the Vcore supply voltage eliminates this problem and, when set by a precision ADC and reference combination, results in a solution that is stable over operating conditions, including voltage input, temperature and process variations.

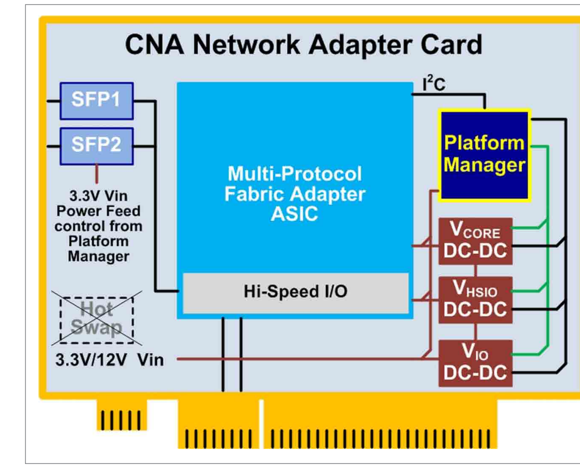


*Figure 2: Converged Network Adapter Voltage Scaling Solution*

Interfacing with a wide variety of DC-DC converters is simplified through the use of design software such as Lattice's PAC-Designer. All required external components (resistors) are computed and determined in advance for optimum control over all DC-DC converter errors. When placed under Platform Manager closed loop control, a power supply's errors are reduced to less than 10mV max error Vout. Designers simply specify what operational voltages they want achieved by various DC-DC outputs and software chooses all the necessary external components and internal device settings to achieve precision trimming of the external power supplies. As various supplies are used again in successive designs, they are captured in a DC-DC component library for reuse, further easing the design task.

A Flexible I2C interface including general purpose I/O (GPIO) that can be programmed to interface directly with proprietary voltage scaling circuitry is now being included in some advanced digital processing engine ASICs and other ICs found in modern circuit board electronics. A device such as the Platform Manager can easily accept these control signals from the advanced ASIC, eliminating the need for an external power supply controller. Instead, this function becomes part of the device's tightly integrated solution.

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# HIGH-SPEED SYSTEMS POSE MANY POWER DESIGN CHALLENGES

By David G. Morrison, Editor, How2Power.com

Power converters rated in the hundreds or even thousands of megawatts. Overhead lines and undersea cables running as long as a couple thousand kilometers. Equipment operating lifetimes measured in decades. Billion dollar budgets.

Many discussions about power system design focus on fundamental challenges such as the quest for greater power supply efficiency or the improvements made possible by advances in power component technologies, circuits, or topologies. However, power system design is also impacted by the many advances and changes in technology on the application side. For many designers, there are growing challenges in the design of power supplies for high-speed circuits, both those encountered in RF systems and in high-speed digital logic designs.

I recently spoke with Steve Sandler about the issues power designers need to consider when powering RF and high-speed digital circuits. As a chief engineer with AEi Systems, Sandler has developed extensive expertise in the design and analysis of both power and RF systems. Sandler is also the managing director of Picotest, a company specializing in precision test and measurement equipment, and as such many of the issues he raises concern test and measurement of both power and RF systems.

Since the issues are wide-ranging, Sandler compiled a list of the top 10 considerations for power designers working with RF or high-speed digital applications:

1) In both RF and digital designs the load can change very quickly. "In some cases, the power supply will be required to transition from full load to no load or no load to full load in a single clock cycle, which can be less than 5 ns or even much less with newer FPGAs," says Sandler. This leads to significant signal integrity type issues, and creates significant concern over parasitics such as ESL in capacitors.

2) Digital and RF designs often use very complex filters on the voltage regulators. Sandler comments that while these filters may be necessary, it is important that designers understand their impact on stability and also on output impedance. In many cases, these filters include RF "beads," presenting a dc-bias-dependent inductance that can also degrade both stability and impedance.

3) Most of these systems employ a distributed power architecture, meaning that several regulators are connected to one source. "This configuration is impacted by regulator PSRR, crosstalk and reverse transfer through the

regulators," says Sandler. Crosstalk is the result of the reverse transfer of one regulator creating a voltage at the common source, where it then is distributed through the PSRR of other regulators.

4) Low phase margin (<30 degrees at end of life) is not just a number. At margins below 45 degrees, the performance of PSRR, reverse transfer, dynamic regulation and output impedance are all degraded. Therefore, designers must observe industry-best practices for minimum end-of-life phase margin, he says. Additionally poor stability results in phase discontinuities and high Q resonances, which can significantly degrade the jitter of ADC clocks. This jitter than impacts the performance of the ADC.

5) While linear regulators are frequently viewed as the low-noise alternative to switching regulators, Sandler observes that low dropout regulators (LDOs) are generally noisy, especially at lower frequencies. "Low noise amplifiers (LNAs) and high-speed clocks generally cannot tolerate the noise or the poor power supply rejection ratio (PSRR) resulting from them."

6) Sandler also points to another issue arising with linear regulators. "We often find linear regulators have multiple 0-dB gain crossings, with the highest in the megahertz to tens of megahertz," he says. "This is generally due to the distance of the capacitors away from the regulators and the ESL associated with tantalum capacitors." Another capacitor-related issue: PSRR is often degraded by the addition of an input capacitor, according to Sandler.

7) Linear regulator bandwidth is another consideration because, says Sandler, it is "generally highly load dependent. Low phase margin results in ringing and the load variations modulate the ringing. The end effect is simultaneous amplitude and frequency modulated supply lines. RF circuits REALLY don't like that." This is generally most significant at the lowest operating currents.

8) For designers tempted to overlook board-level parasitics, Sandler offers the following note of caution. "Voltage regulators for RF often need the printed circuit board parasitic included in assessments. Often the PCB capacitance will drive the results of PSRR and other sensitive characteristics."

9) As noted previously, powering RF systems requires a special attention to test issues. "It is best to measure the performance of the power system IN THE SYSTEM and with the SYSTEM operational," explains Sandler. "A few carefully placed test points and the appropriate signal injectors can facilitate these measurements." Measuring in this way includes the effects of the printed circuit board and component parasitics as well as operating into the actual load current and impedance. Electronic loads often interfere with the measurements as they can be very capacitive.

10) Another test-related concern arises in the assessment of the power system's phase margin. According to Sandler, designers need to remember that "it is possible to assess the phase margin of a fixed regulator or a regulator that does not allow access to the control loop." This can be done using output impedance and group delay measurements, which are made possible by certain network analyzers and a particular small-signal current injector, which are now available on the market.

These ten points are by no means an exhaustive list of power design considerations when powering high-speed systems, but rather a starting point in the effort to develop an effective power system. Keeping these issues in mind, engineers may avoid some of the problems that can sidetrack project development or stymie efforts to achieve system performance goals.

**About the Author**

David G. Morrison is the editor of How2Power.com, a free portal providing information on all aspects of power conversion. Morrison is also the editor of How2Power Today, a free monthly newsletter presenting design techniques for power conversion, new power components, and career opportunities in power electronics. Subscribe to the newsletter by visiting www.how2power.com/newsletters

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# NORTH AMERICA UP IN SOLAR

*By Cliff Keys, Editorial Director & Editor-in-Chief, Power Systems Design*

After two years at the top, Germany this year is likely to lose its place as the world's top photovoltaic (PV) solar market, slipping to No. 2 behind former runner-up Italy, according to an IHS iSuppli PV Market Brief report from information and analysis provider IHS (NYSE: IHS).

Following in the wake of the two giant European players will be the United States in third place, with 2.7 GW worth of installations in 2011; China in fourth, with 1.7 GW; Japan in fifth with 1.3 GW and France in sixth with approximately 1.0 GW of new installations.

Despite the worldwide increase in new PV installations this year, component prices in the solar supply chain—stretching from wafers to modules—are on the decline. In the third quarter, for instance, large PV systems were being offered in Germany at 1.60 euros—or about $2.13—per watt, down from 1.80 euros; with residential rooftop installations also declining to 1.90 euros, a reduction from 2.20 euros.

PV solar system installations in Germany during 2011 are expected to decline to 5.9 gigawatts (GW), down 20 percent from 7.4 GW in 2010. Meanwhile, Italy in 2011 is set to install up to 6.9 GW worth of PV systems, nearly double the 3.6 GW from 2010.

It is reported that propelled by residential and institutional investors who support green initiatives as well as sustainable funding, Germany has been the world's leading country for PV installations since 2009

New PV solar installations in Germany in the first half of 2011 amounted to only 1.7 GW—less than a third of total for the entire year. High PV module prices early in the year caused buyers to hold off purchases until costs moderated. However, figures from the German Grid Agency reported installations of 2.3 GW from June to September, exceeding the original IHS estimate of 2.2 GW. A mini boom also materialized in Germany in October, November and December because of reduced system prices and changes of tariffs expected in January 2012.

Meanwhile, Italy this year added more solar capacity than any other country. Following the two giant European players will be the United States in third place, with 2.7 GW worth of installations in 2011; China in fourth, with 1.7 GW; Japan in fifth with 1.3 GW and France in sixth with approximately 1.0 GW of new installations. It should be an interesting time for North America.

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