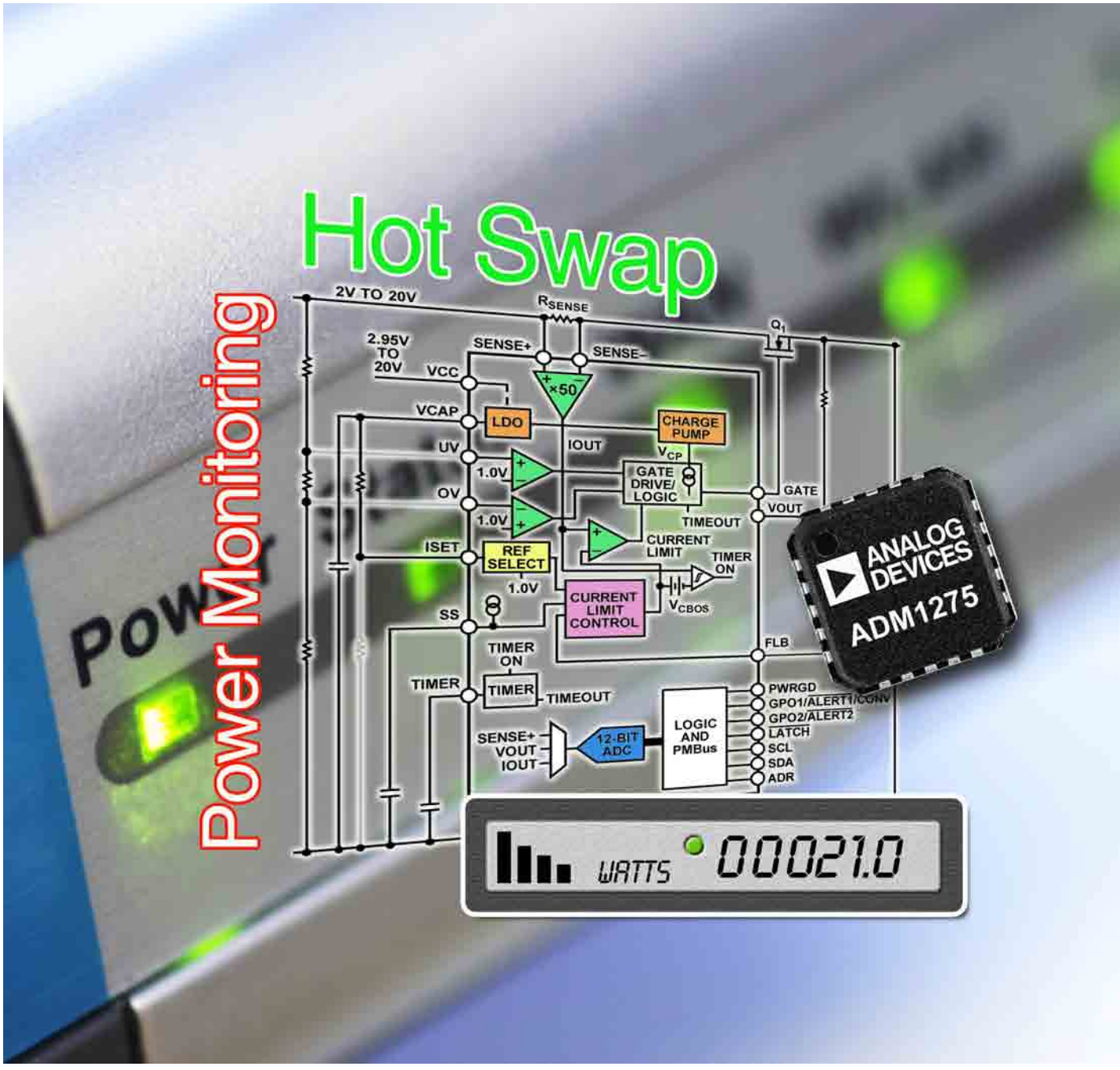
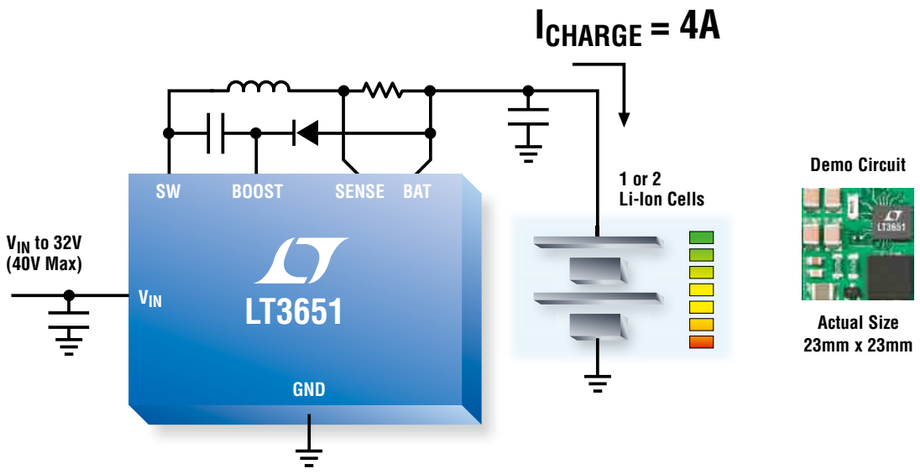
PSD EUROPE
Power Systems Design: Empowering Global Innovation
April 2011




SPECIAL REPORT: WHITE GOODS (PG 41)

# Charge BIG Batteries Fast



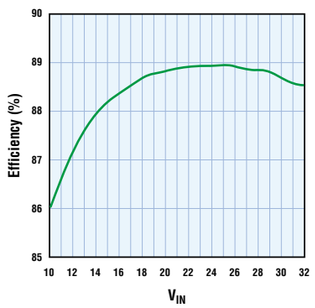

## High Voltage, High Current, High Efficiency Charger

The LT®3651 enables fast charging of Li-Ion/Polymer batteries by delivering up to 4A of continuous charge current with minimal power loss. This is due to its high efficiency switchmode topology, including on-chip synchronous MOSFETs. Its autonomous operation means no microcontroller is necessary and the device integrates an onboard C/10 or timer charge termination. The LT3651's programmable input current limit with PowerPath™ control regulates charge current to maintain a constant supply current, preventing the input supply from collapsing.

### Features

- Charge Current up to 4A
- Wide Input Voltage Range: 4.8V to 32V (40V Max)
- Programmable Switching Frequency: 200kHz to 1MHz
- C/10 or Timer Onboard Charge Termination
- High Efficiency Operation Minimizes Power Loss
- Programmable Input Current Limit
- Compact 5mm x 6mm QFN Package

### Efficiency vs $V_{IN}$




### Info & Free Samples

www.linear.com/3651

+49-89-962455-0

Free Battery Charger Solutions Brochure

www.linear.com/batsolutions



***Europe Sales offices:*** **France** 33-1-41079555 **Italy** 39-02-38093656 **Germany** 49-89-9624550 **Sweden** 46-8-623-1600 UK 44-1628-477066 **Finland** 358-9-88733699 ***Distributors:*** **Belguim** *ACAL* 32-0-2-7205983 **Finland** *Tech Data* 358-9-88733382 **France** *Arrow Electronique* 33-1-49-784978, *Tekelec Airtronic* 33-1-56302425 **Germany** *Insight* 49-89-611080, ***Setron*** 49-531-80980 **Ireland** *MEMEC* 353-61-411842 **Israel** *Avnet Components* 972-9-778-0351 **Italy** *Silverstar* 39-02-66125-1 **Netherlands** *ACAL* 31-0-402502602 **Spain** *Arrow* 34-91-304-3040 **Turkey** *Arrow Elektronik* 90-216-4645090 **UK** *Arrow Electronics* 44-1234-791719, *Insight Memec* 44-1296-330061

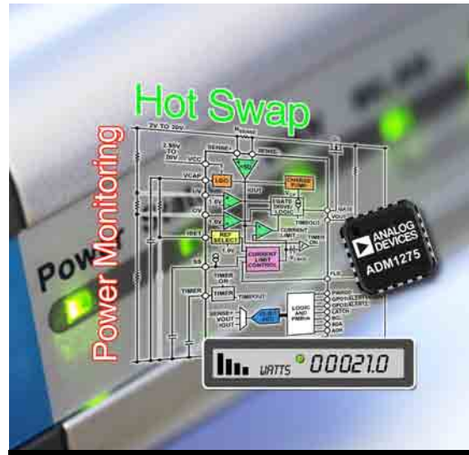
LINEAR TECHNOLOGY

PSD EUROPE
Power Systems Design: Empowering Global Innovation

WWW.POWERSYSTEMSDESIGN.COM

Visit us online for exclusive content; Industry News, Products, Reviews, and full PSD archives and back issues






**COVER STORY**
High Power Systems (pg 13)

Highlighted Products News, Industry News and more web-only content, to:
**www.powersystemsdesign.com**



PSD EUROPE

**AGS Media Group**
146 Charles Street
Annapolis, MD 21401 USATel:
+410.295.0177
Fax: +510.217.3608
www.powersystemsdesign.com

**Editor-in-Chief**
Cliff Keys
*cliff.keys@powersystemsdesign.com*

**Contributing Editors**

Liu Hong, Editor-in-Chief, Power Systems Design China
*powersdc@126.com*

Ash Sharma, IMS Research
ash.*sharma@imsresearch.com*

Dr. Ray Ridley, Ridley *Engineering*
*rridley@ridleyengineerng.com*

David Morrison, How2Power
*david@how2power.com*

**Publishing Director**
Jim Graham
*jim.graham@powersystemsdesign.com*

**Publisher**
Julia Stocks
*julia.stocks@powersystemsdesign.com*

**Circulation Management**
Kathryn Philips
*kathryn.phillips@powersystemsdesign.com*

**Research Director**
Meghan Corneal
meghan.corneal@*powersystemsdesign.com*

**Magazine Design**
Louis C. Geiger
*louis@agencyofrecord.com*

**Production Manager**
Chris Corneal
*chris.corneal@powersystemsdesign.com*

Registration of copyright: January 2004
ISSN number: 1613-6365



Volume 8, Issue 2

# WHITE GOODS AND WOES

Welcome to this issue of PSD where we carry a feature section on white goods and domestic appliances. In former times these devices had no regard for energy efficiency or, in the case of motorized appliances, the noise they generated. These days are fast coming to an end. Regulations are ever tightening and consumers themselves are now becoming more concerned with the energy they consume – both from a cost and from an environmental standpoint. This is driving manufacturers of these appliances to demand better methods of power and motor control which, in turn, normally requires more sophisticated power and control management in the development of modern, consumer-friendly products.

For the world's semiconductor suppliers, after six consecutive quarters of sequential growth, the fourth quarter of 2010 saw revenue contract by 3.7% over the previous period—the first quarterly retreat since the beginning of 2009—according to new research from IHS iSuppli. Revenues for the 298 semiconductor suppliers tracked by the IHS iSuppli Competitive Landscaping Tool (CLT) fell to $77.2 billion in the fourth quarter of 2010, down from $80.1 billion in the earlier quarter. But this depressed revenue was still 11.9% higher than the fourth quarter of 2009. Despite the fourth-quarter contraction, semiconductor revenues surged by $74.5 billion in 2010, setting a new record and surpassing the prior record increase during the dot-com bubble of 2000.

Apple fans are no-doubt aware that the company has managed to significantly reduce the thickness and weight of the iPad 2 by trimming the dimensions of several key components, most notably the battery, a teardown analysis by IHS iSuppli has revealed. This reduction in thickness of the battery subsystem is due to Apple moving from two thicker cells to three thinner ones, flattening out the entire battery structure.
This refinement to the design spurred a 10-15% increase in its iPad 2 power-density, which is a measure of battery life relative to the mass of the battery. It shrinks the iPad 2's weight by 5 grams, while still delivering the same battery lifetime.

The absolute horror of the earthquake in Japan, already well reported, certainly will continue to cause disruption to the global electronics market and has the potential to greatly impact the whole technology industry. We wish the people of that great nation well and will leave the daily reports to those best qualified.

I hope you enjoy our new look and especially our new, user-designed website which is updated on a real-time basis. Check out the community section, naturally after our fun strip, Dilbert, at the back of the magazine. Thank you for your extremely helpful feedback, and please keep it coming.

All the best,

**Cliff**
Editorial Director & Editor-in-Chief
Power System Design
Cliff.Keys@powersystemsdesign.com





# IR'S NEW FAMILY OF PFC ICs

International Rectifier, has introduced the IR115x family of µPFC™ power factor correction (PFC) ICs for a wide variety of AC-DC applications including lighting, LCD/PDP TV and game consoles, fans, air conditioners, uninterruptible power supplies (UPS) and Switch Mode Power Supplies (SMPS), ranging from 300W to 8kW.


The IR115x ICs, utilizing IR's One Cycle Control (OCC) technology, offer high power factor (PF), low total harmonic distortion (THD) and excellent DC Bus regulation while enabling drastic reduction in component count, PCB area and design time compared to traditional solutions. The ICs are designed to operate in continuous conduction mode Boost PFC converters with average current mode control over 85-264VAC input line voltage range.

By integrating more features than traditional PFC solutions and eliminating the need for external implementation, the IR115x significantly reduces the overall cost and complexity of a feature-rich PFC control design compared to traditional PFC solutions while offering enhanced protection and safety.

The new µPFC™ ICs offer advanced system-enabling and protective features including dedicated pin for over-voltage protection, cycle by cycle peak current limitation, open loop protection, VCC UVLO and programmable soft-start. The user initiated micropower startup/sleep-mode enables compliance with standby power requirements mandated by regulations such as Energy Star, Green Power and Blue Angel. The IR1152S and IR1153S also feature brown-out protection.

The IR1155S offers programmable switching frequency between 48 kHz to 200 kHz based on the specific application requirement, while the IR1153S offer fixed switching frequency of 22.2kHz. All these devices are compatible with IR's Ultrafast and Warp IGBTs for systems with power ratings higher than 750 Watt and switching frequency up to 100kHz.

The devices are lead free and RoHS compliant. Datasheets, overviews application notes and online design tools are available on the International Rectifier website. The IRAC1152-350W and IRAC1155-300W reference designs, demonstrating the design of a universal input 350W AC-DC Boost PFC Converter, are also available. Design & layout tips are included.

www.irf.com

# WHITE & CONSUMER GOODS

Reported By Cliff Keys

With these goods becoming more energy efficient as a function of regulations and consumer demand coupled with the need to add more functionality, manufacturers are hard-pressed to differentiate their products and in finding the space to pack it all in. I talked with Wisam Moussa, Global lead of FAE for Murata Power Solutions.

Naturally, there are sophisticated chips around that can control the motorized parts of today's domestic appliances and there are many solutions around to do this. The area often neglected, or at least left to the last phase of development, is the heart of any system; the power supply. This phase of the product design is not so simple. It must take up the smallest space, be highly efficient and completely reliable under a variety of often harsh environments. On top of this is the need to consider safety and isolation. All these features add to the cost, but these days manufacturers who want to deliver a high quality product, with a reliable and long maintenance-free life are willing to make this investment. Apart from the performance enhancement, the reputation of the manufacturer can then enter the realms of a 'quality brand'.

Designing a tiny DC/DC converter that meets these performance expectations and that provides a degree of future-proofing is not straightforward. The first challenge is to select a topology that meets the size constraints that miniaturisation demands, yet is capable of adequate output power delivery, isolation and regulation. The chosen approach should be able to address a range of common input and output voltages as well as ideally being extensible to deliver more power from a similar platform.

Power engineers are under constant stress to deliver on time and 'right first time' to meet market entry deadlines. Often with little time to tweak and fine-tune a circuit, the safest solution, and the most cost-effective when considering the potential cost of redesign or spins is to choose a fully optimized module that is virtually guaranteed to work first time.

Power manufacturers, by combining proprietary circuit enhancements and recent component fabrication techniques, can improve the load regulation of a converter. For example, Murata Power Solutions' engineers were able to increase their MTU1 part's load regulation performance to a maximum -4, +5.5% from 10% of full load upwards. By comparison, previous ranges achieved -7.5, +10%. For many applications, the load regulation these enhancements offer obviates the need for inefficient and space-hungry linear post-regulation stages.

These efficiency improvements translate into an approximately 56% reduction in internal power dissipation that reduces internal hot-spots maximising reliability while minimising the heat load that the host equipment has to accommodate. The MTU1 series requires no derating over its -40 to +85°C operating range. Also the reduced capacitance further isolates input and output, making the part far less susceptible to transmitting noise through its isolation barrier which could potentially disturb sensitive loads.

But the most dramatic improvement that the MTU1 series introduces is the part's new footprint, which shrinks the 12.70 x 11.70mm pad land pattern that industry-standard parts use to just 9.10 x 6.08mm. This represents a footprint area over the new device's pins of 0.69 cm2 and an effective power density of 1.71W/cm3 for a cube-like outline that measures 8.2 x 8.4 x 8.5mm.

Significantly - and unlike some plastic-encapsulated packages that industry-standard components employ - the MTU1's composite assembly has a level 1 rating for moisture sensitivity (MSL1).

The power engineer's job is not an easy one. By utilizing this technology, especially in the example of white and consumer goods used here, designers can avoid the problems that plague many manufacturers' brands further down the line.

www.murata-ps.com

# ENERGY CONSERVATION EFFORTS DRIVE APPLIANCE INNOVATION

By Elizabeth Cruz

As the price of energy continues to rise, regulatory bodies around the world are continuously looking for new ways to reduce electricity consumption. New and tougher energy efficiency regulations are being introduced and these offer interesting opportunities for new technologies in home appliances.

The EU's Energy Label has added three classes on top of the previous highest efficiency band; China continues to push minimum energy requirements for room air-conditioners and cold appliances, and the US's Energy Star program is driving major reductions in energy use for most appliance types. These more stringent standards are helping to stimulate design changes in a traditionally conservative market.

In Europe, over 90% of appliances sold are in the "A" class of the EU Energy Label scheme, which tells consumers how efficient an appliance is and therefore how much can be saved on their electric bills. In 2010, the EU approved three new energy classes beyond "A" that will go into effect for washing machines and dishwashers, which must also include noise declarations for these appliances. Additional regulations from the EU, under the Ecodesign Directive, are aimed at limiting stand-by and off-mode power losses. By 2013, certain appliances will be required to use less than 0.5 watts of energy in off-mode, affecting the design of user interfaces, auxiliary power supplies and input filters.

The growth of a middle-class in China has been accompanied by a major increase in ownership of home appliances and in residential electricity use. In 2010 the National Development and Reform Commission of China (NDRC) increased the minimum energy efficiency requirements for room air conditioners by 23% from the previous standard. R oom air conditioners, which account for roughly one-fifth of energy demand in China, are becoming more efficient by using inverter-based variable speed drives to control the compressor and sometimes also the motor running the fans in the unit. The regulation is aimed at saving around 636 billion kilowatt hours of electricity annually.

The US is also raising energy efficiency standards as the potential for energy savings through technology increases. Proposed changes to the Energy Star program (slated to take effect in 2014/2015) will call for a reduction of energy use in refrigerators and freezers by 30%, clothes washer efficiency increases of 26% to 43% for top and front loading respectively, and room air conditioner efficiency increases of up to a 15%. By 2013 dishwasher manufacturers will be called to increase efficiency by 14% and reduce water consumption by 23%. The introduction of more accurate pressure sensor technology, capable of measuring water levels in the drum to an accuracy of less than 1 millimeter, is an effective tool in reducing unnecessary water use.

The above examples of tightening regional energy standards underline the potential for innovations in electronics design in white goods. The appliance industry has traditionally been slow to adopt new technology, but with growing demands on appliance makers to reduce energy consumption, this is changing. New technologies and uses for motor control, power supplies, sensors and more will increasingly have a place in major home appliances.

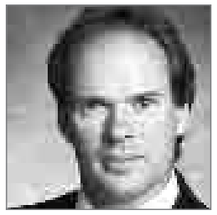
Advanced motor control is now advancing aggressively in some appliance types such as room air conditioners and dishwashers. Further increases in adoption are foreseen in the next five years, particularly in washing machines and refrigeration. Together with greater innovation in the design of user interfaces, these trends will maintain the interest of semiconductor and component companies in the home appliance market over the next five years.

*Author: Elizabeth Cruz*
*Market Analyst, Power & Energy-Appliances*
*IMS Research*

www.imsresearch.com

# POWER SUPPLY DEVELOPMENT DIARY

## Part XII



By Dr. Ray Ridley

This article continues the series in which Dr. Ridley documents the processes involved in taking a power supply from the initial design to the full-power prototype. Parts X and XI of this series of articles presented the first seven rules for good PC board layout. Part XII finishes up the design rules for good PCB layout design, focusing on the judicious use of planes.

**PCB Layout Rule 8: Use Planes to Capture Noise**

Switching power supplies generate high-frequency waveforms with both high-frequency and high-amplitude current and voltage pulses. In the last article of this series, it was shown how to keep current loops small in order to minimize leakage inductance and magnetic EMI generation. This is an essential step since shielding of magnetically-generated noise is difficult. It is better not to generate it in the first place, hence the need to close the high-frequency current loops.

Noise is also generated by electrostatic antennae created by the power supply components. Nodes which have high-frequency voltage waveforms, when coupled with large-area components or heatsinks, will generate considerable amounts of EMI.

Figure 1 shows the basic schematic of the forward converter with a single output. The worst electrostatic noise generators are shown in blue, red, and purple. These are the nodes of the circuit with the highest dv/dt waveforms. Typically, the waveform shown in red is the worst offender since it is tied to the large surface area of the drain of the lower power FET.

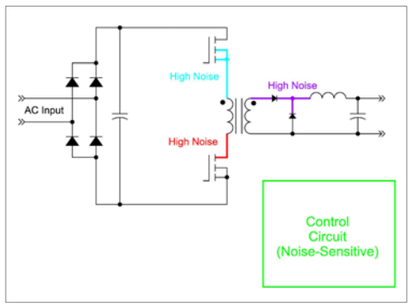



*Figure 1: Forward Converter Schematic showing Electrostatic Noise Generators*

Shielding planes can be used to greatly reduce the effect of these noise-generating nodes. Three such planes are shown in Figure 2. These can be implemented in the PC board, if space and available layers allows, and if the power components are surface mounted. The planes should be tied to local RF ground points, such as the return of the main power rail on the input, or the return of the output voltage.

Notice that there is no plane for the source of the upper FET since this is normally self-shielding due to the layout of the power packages. The substrate of most FETs are connected to the drain of the FET. The upper FET is connected to an RF ground point on the positive side of the input rail.

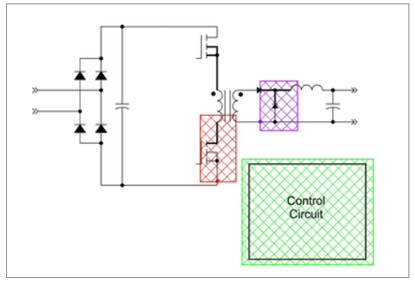



*Figure 2: Shields for Collection of Electrostatic Noise (Red and Purple) and for Control Circuit Shielding (Green). Colored Dots Show Where Shields are Connected.*

If the power components are through-hole mounted, the use of planes to collect EMI in the PCB will be of limited value. In this case, the heatsinks of the power components themselves should be locally grounded, ensuring that they have suitable voltage isolation from the power devices.

**Layout Rule 9: Use Planes to Shield from Noise**

PWM controllers can be very sensitive to noise, and must be protected to ensure proper operation. Stray noise into the ports of high-gain operational amplifiers and comparators can lead to catastrophic failures of power supplies. Even the simple act of applying an oscilloscope probe improperly to a control circuit can result in failure of a switching power supply.

It is highly advisable to provide a ground plane underneath the area of the control chip and its surrounding components. This will establish a low-impedance ground connection to all parts of the control circuit, and minimize any EMI pickup loops and stray inductance that may cause problems. The ground plane used to shield the control circuit should be tied properly to the return of the main output if this is referred to the same ground. A single connection should be provided to connect the two common points as shown in Figure 3.

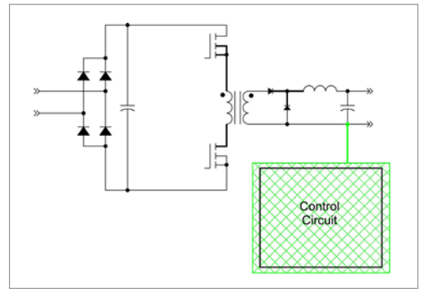



*Figure 3: Tying the Ground Plane to a Single Point on the Main Output*

If extra layers are available on the PCB, it can be tempting to pour a ground plane over much larger areas in order to reduce noise. However this can have the effect of degrading the integrity of the ground in the quiet areas of the circuit. For example, if a ground plane is placed on the PCB as shown in Figure 4, noise problems can result. The high-frequency pulsating currents in the secondary will flow through parts of the ground plane, and this can disturb noise-sensitive components.

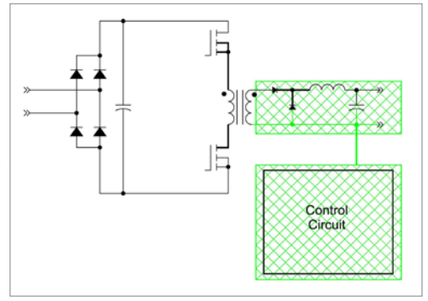



*Figure 5: Two Separate Ground Planes Achieve Noise Shielding and Proper Ground Integrity*

A better layout for ground planes is illustrated in Figure 5. The upper part of the plane is used for two purposes – first, to shield the electrostatic noise generated by the output rectifiers (shown in purple in Figure 1), and secondly, to provide a large conduction area for the ground of the output with low impedance.

The lower part of the plane is used just to keep the noise from interfering with the control circuit. None of the high-frequency or high-current waveforms are allowed to flow through this part of the ground plane. This preserves the integrity of the ground. The two separate

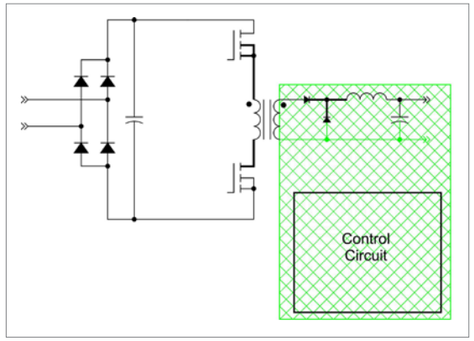



*Figure 4: Using a Single Ground Plane can Degrade Ground Integrity*

parts of the plane are connected by a single trace on the PCB.

**Layer Choices for PCB Planes**

If you have two or more layers on the PCB, you have choices as to where to put the shielding planes. There are several design philosophies that may be used in choosing where you put the plane layers.

I always like to have access to all the trace routings in order to be able to see all of the waveform nodes, and sometimes to make changes on the early iterations of the PCB. For complicated boards, this can tie up the top and bottom layers of the circuit board, requiring the ground and shield planes to be placed internally. With simpler circuits, most of the traces can often be placed on one side of a double-sided board, leaving the other free for planes.

Another convenient choice is to put the ground plane under the control circuitry on the top layer of the PCB. This provides a local ground connection for probing the circuit with short lead lengths. If you are using SMT components, you will not be able to put a plane on that same layer if the component density is high.

The resulting compromise solution is to place each plane individually, taking care of functionality and practical aspects at the same time. There is no single optimal solution for every design. Think carefully about the role of each part of a plane. With a two-layer board, a good solution can usually be found.

The outline of the planes should be placed on the board manually, thinking carefully about the components that need to be shielded from either generating or being susceptible to noise. Once the CAD system has filled in the area of the plane, ensure that all parts of the plane are properly connected and that isolated islands and long connections have not been inadvertently generated. Occasionally, traces will need to be rerouted to keep the planes reasonably intact.

It is important not to just pour planes across the entire expanse of the board, even if the layers and space are available. Planes that are designed to protect sensitive circuits should not be continued in the areas where there are noisy components, or they may do more harm than good.

**Summary**

The last few articles of this series have shown the nine critical rules for good PC board layout. The last step, placing power and ground planes for EMI control, is a process that involves intimate knowledge of the operation of the power circuit, and cannot be automated. It takes a lot of experience to do this effectively. Following these nine critical rules will help achieve good results on your first boards. Laying out a good circuit board for power supply design is a skill that takes years to acquire, and the time-consuming nature of this task should never be underestimated. With each new power supply design, anticipate at least two iterations of the PC board. This is true even if there are no changes to the circuit schematic.

If you are new to power supply design, it is highly recommended to begin to learn the art and science of power supply board layout as early in your career as possible. This is a very valuable skill that will greatly increase effectiveness as a power designer.

**References**

"Power Supply Development Diary Parts I-XI", Ray Ridley, Power Systems Design Magazine, 2010.

*Author: Dr. Ray Ridley*
*President*
*Ridley Engineering*

www.ridleyengineering.com





# HIGH POWER SYSTEMS

## High accuracy Hot-Swap and power monitoring

By Marcus O'Sullivan

Many high power systems require the use of a hot-swap device to safely control of the inrush currents at powerup and provide fault protection.

These circuits are commonly found in systems such as servers, network switches, redundant-array-of-independent-disk (RAID) storage, and other forms of communications infrastructure that need to remain fully operational through their working life. These systems are known as high-availability systems. In the event of a component failure, the component will need to be removed from the system and replaced with a fully functional component, all while the power remains on and system remains operational. This process is known as hot swapping, or hot plugging.

In order to safely facilitate this event, a hot-swap controller is required to control the inrush current and prevent interruption of the backplane supply to other systems. During normal operation the controller also provides protection against short circuits and other overcurrent faults. Analog Devices latest range of hot-swap controllers, also integrate a high accuracy digital power monitor which can facilitate high accuracy system power metering. See Figure 1.

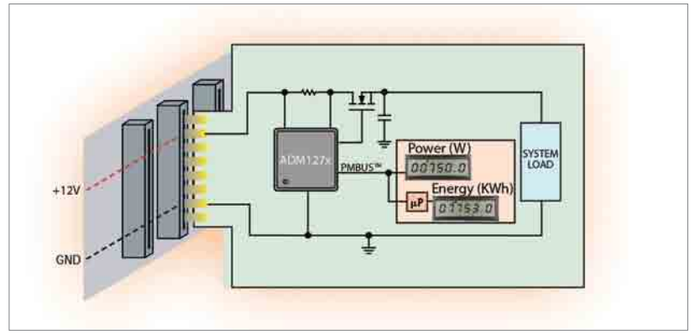



*Figure 1*

As the power requirements for these systems are growing, efficiency is becoming more significant. Also the practicality of designing around loose tolerance and high insertion power loss is becoming more difficult. The ADM1275 not only provides high accuracy power monitoring to report the system power, but also has many features specifically designed to reduce the losses typically associated with hot-swap, such as insertion losses of sense resistors and MOSFETs.

Let's look at the design process, including component selection considerations, for a typical high current blade server hot-swap design.

**System Specifications**

The following conditions are

assumed for this example:

- Controller = ADM1275
- VIN = 12 V Nominal
- VMAX = 12.6 V
- ITRIP = ~70 A
- CLOAD = 5000 µF
- TAMAX = 65°C
- RPOWERUP = 10Ω (static load resistance during system power up)

To simplify this example, the calculations exclude many component tolerances. These tolerances should of course be considered when designing for worst-case conditions.

**Sense Resistor Selection**

The sense resistor chosen is primarily based on the required circuit breaker trip current. However, the ADM1275 also includes an adjustable current limit threshold which allows for fine tuning of the current limit beyond that provided by the limited availability of standard sense resistor values. The sense voltage can be programmed within a 5mV to 25mV range. Such a low sense voltage, along with the flexibility of programmability, offers reduced power loss and size in sense resistor selection.

The circuit breaker timer (current fault glitch filter) begins is typically 0.8mV below the regulation point. This means that to set a trip point of 70A(19.2mV) we need to set the regulation point to ~73A (20mV).

This is not a common available

$$R_{SENSE} = \frac{V_{SENSE}}{I_{TRIP}} = \frac{0.020\ \text{V}}{73\ \text{A}} \approx 0.273 m\Omega$$

value so the closest to consider is 0.25mΩ, with 2x 0.5mΩ in parallel. Lets reverse the equation above to determine the required sense voltage.

$$V_{SENSE} = R_{SENSE} \times I_{TRIP}$$
$$= 0.25 m\Omega \times 73 \approx 18.25 mV$$

The ISET pin can be programmed to a desired voltage using a divider from the VCAP reference. See Figure 2. ISET voltage = Vsense x 50.

$$V_{ISET} = V_{SENSE} \times 50 = 18.3 mV \times 50 = 0.915 V$$

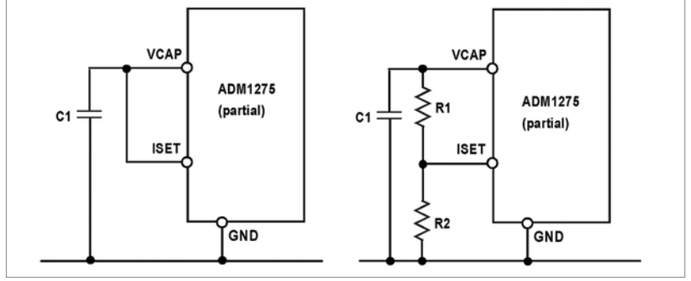



*Figure 2*

Using the VCAP reference of 2.7V and assuming R1= 100kΩ, this will result in a bottom resistor of 51.1kΩ. The given ISET voltage provides a circuit breaker trip point of ~70A and a regulation current set point of 73A.

Assuming worst case DC current could be as high as 75A (including tolerances), the maximum DC current for each resistor can be given as ~42A, including ~10% to account for imbalance.

**Therefore power can be calculated as:**

$$P_{RSENSE} = I_{TRIP}^{2} \times R_{SENSE}$$
$$= (42\ \text{A})^2 \times 0.0005\ \Omega$$
$$= \sim 0.882\ \text{W}$$

So each sense resistor should be capable of dissipating >1 W (including temperature derating factors). A 2W or 3W resistor is recommended to reduce running temperatures.

A series of 10Ω resistors should be used to average all these nodes together to the controller.

**Summary of the key component selection for this section**

RISET(TOP) = 100 kΩ
RISET(BOT) = 51.1 kΩ
RSENSEx = 0.5mΩ x2 (2 / 3W)
RAVGx = 10Ω x4

**MOSFET Selection**

The first consideration as criteria for selection of a suitable MOSFET is the RDSON specification, to ensure that minimum power is lost in the MOSFET when it is fully enhanced in normal operation. The ADM1275 features a high

voltage gate drive to ensure a minimum of 10V VGS is achieved to maintain the lowest specified RDSON. The gate drive circuit is designed to achieve this while still ensuring the 20V maximum VGS spec is not violated during fault conditions.

As the temperature of the MOSFET increases, its power rating is reduced, or derated. The RDSON spec determines the maximum junction temperature of the MOSFET and therefore the required derating can be applied to SOA parameters. In addition, running MOSFETs at high temperatures may decrease their reliability.

Let's begin by estimating the required RDSON. Recall the maximum DC current was 75A, worst case. Then using the maximum ambient temperature specified in section 1 we can estimate the power loss in the MOSFET(s).

First we make a few assumptions:

- RthJA = 40 C/W (maximum)
- TjMAX = 120 °C

(This is the maximum preferred junction temp, keeping well away from any silicon limits)

Calculate the junction temperature rise:

Then the power for a single FET:

$$T_{RISE} = T_{jMAX} - T_{AMAX} = 120 - 60 = 60^{\circ}\text{C}$$

Now total RDSON:

$$P_{MOSFET} = \frac{T_{RISE}}{R_{thJA}} = \frac{60}{40} = 1.5W$$

This number is far too small for

$$R_{DSON} = \frac{P_{MOSFET}}{I_{MAXDC}^{\ 2}} = \frac{1.5}{75^2} = 0.266m\Omega$$

a single FET so let's try 3 FETs in parallel:

Now we subtract 10% to give us

$$R_{DSON} = \frac{P_{MOSFET}}{(I_{MAXDC}/3)^2} = \frac{1.5}{25^2} = 2.4m\Omega$$

some margin for imbalance due to layout asymmetry and a further 1.4 factor to allow some derate:

$$R_{DSON} = \frac{2.4 \times 0.9}{1.4} = 1.5m\Omega$$

Taking this as our target RSDON we can now search for suitable candidates. The search can be narrowed to FETs that fit the following profile:

- VDS = 25/30V (20V may be possible but not preferred)
- VGS = 20V
- RDSON ≤ 1.4mΩ

After selecting a suitable MOSFET, the derating of the RDSON should be quantified using the MOSFET datasheet graph of RDSON against TJ.

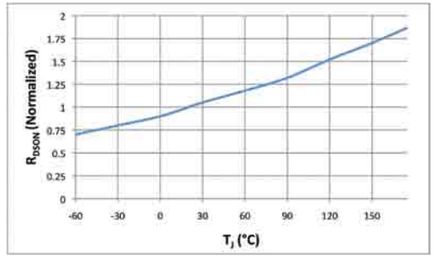



*Figure 3*

Using TjMAX of 120 °C, we can see from Figure 3. the RDSON increases by a factor of ~1.52, to about 1.824mΩ (assuming 1.2mΩ at 25°C) at 120°C. As a rule its preferred to keep junction temp ≤120C to increase reliability.

Assuming that the MOSFET's max RDSON is 1.83mΩ, the power of each FET can be:

$$P_{MOSFET} = \left(\frac{I_{MAXDC}}{n} + 10\%\right)^2 \times R_{DSON}$$
$$= (27.5\,\text{A})^2 \times 0.00183\,\Omega$$
$$\approx 1.39\text{W}$$

This is determined by the MOSFET's thermal resistance at ambient temperature should be specified in the datasheet. The footprint size, airflow, nearby heat sources and additional copper will also have an effect on this value so care must be taken to ensure the specified conditions are met. Assume, for this design a target of:

$$R_{thJA} = 40^{\circ}\text{C/W}$$

(Note: Care should be taken to ensure layout/airflow does not exceed this figure)

As the MOSFET is expected to dissipate ~1.39W, a worst-case temperature rise of 55.6°C above ambient can be expected as follows:

$$T_{RISE} = R_{thJA} \times P_{MOSFET} = 55.6^{\circ}\text{C}$$

The resulting junction temp of the FET can be determined as follows:

$$T_J = T_A + T_{RISE} = 60 + 55.6 = 115.6^{\circ}C$$

As this is below the maximum selected value of 120°C, the risk of thermal runway should be avoided. When using multiple MOSFETs in parallel, a 10Ω resistor should be use in series with the gate of each MOSFET to prevent parasitic oscillations.

Summary of the key spec / component selection for this section:
QX = Selected 1.2mΩ MOSFET.
RthJA = 40 k/W
RGATE = 10Ω (x3)

**Power Derating Factor**
Now that the maximum junction temperature is verified we can determine the maximum derate factor. This number will be used to derate all the SOA parameters to verify a robust solution across temperature.

To determine the maximum expected case temperature we can use:

$$T_C = T_j - (R_{thJC} \times P_{MOSFET})$$
$$T_C = 115.6 - (1.0 \times 1.4) = 114.2^{\circ}C$$

Now the derating factor can be calculated as follows:

$$DF = \frac{T_{J\max} - T_{CSOA}}{T_{J\max} - T_{C\max}} = \frac{175^{\circ}C - 25^{\circ}C}{175^{\circ}C - 114.2^{\circ}C} = 2.46$$

Summary of the key spec / component selection for this section:
DF = 2.5

**Foldback**
The ADM1275 utilizes a foldback technique to protect the MOSFETs in the event of overcurrent faults or short circuits. The output voltage is monitored using a divider on the FLB pin and the current limit is adjusted based on the VDS of the MOSFET. An example of this relationship can be seen in Figure 4.

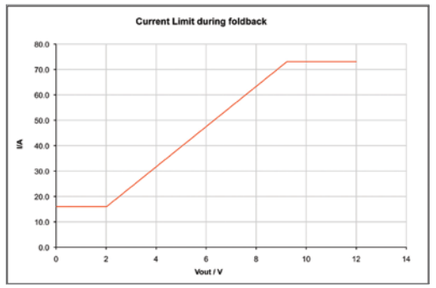


*Figure 4*

When the output voltage is at zero, there is a lower limit clamp to prevent the current limit approaching zero. This clamp is fixed at 0.2V on the FLB pin (or 4mV Vsense), which equated to ~16A on this particular design. As the output voltage increases, the current limit ramps as a function of the output voltage. This threshold is set by the divider on the FLB pin, using a reference equal to VSENSEREG X 50. This voltage should be chosen to be low enough to avoid any expected VOUT load steps from affecting the current limit. The PWRGD output is also derived from the voltage level at the FLB pin.

Targeting 10.3V, we get a divider of 100KΩ top and 12KΩ bottom.
Summary of the key spec / component selection for this section:
VPG = 10.3V
RFLB_TOP = 100kΩ
RFLB_BOT = 12kΩ

**MOSFET Safe Operating Area analysis**
The next step is to review the SOA curve on the MOSFET datasheet to determine how much time it can tolerate the worst case power in the FET. This will determine a suitable timer capacitor value.

In a multiple FET solution, it must be assumed that a single FET could be dissipating 100% of the power during a powerup or vent such as these. This is due to possible differing Vth levels on each FETs, only one could be conducting when in regulation. If a short was applied the Vds of the FET can be assumed to be ~12.6V (assuming source at GND). In reality the number would likely to be lower than this due to line impedance.

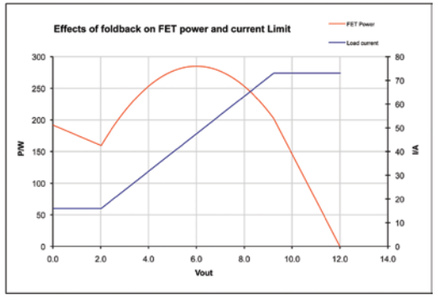


*Figure 5*

However, if we look at the profile

of the FET power against Vout we see that the relationship is not monotonic. See Figure 5.
The worst case power in the FET is shown at approximately 6.3V (50% of Vin). The current can be easily calculated using the following equation:

$$V_{FLB} = V_{OUT\_WCP}\left(\frac{R_{FLB\_BOT}}{R_{FLB\_TOP}+R_{FLB\_BOT}}\right)$$
$$= 6.3\times\left(\frac{12{,}000}{100{,}000+12{,}000}\right) = 0.675$$
$$I_{FLB\_WCP} = \frac{V_{FLB}}{R_{SENSE}\times CS_{GAIN}} = \frac{0.675}{0.25m\Omega\times 50} = 54A$$

(WCP=Worst Case Power)

Now derate this by Derate Factor of 2.5 and we get 135A. So if we go to the SOA diagram of the

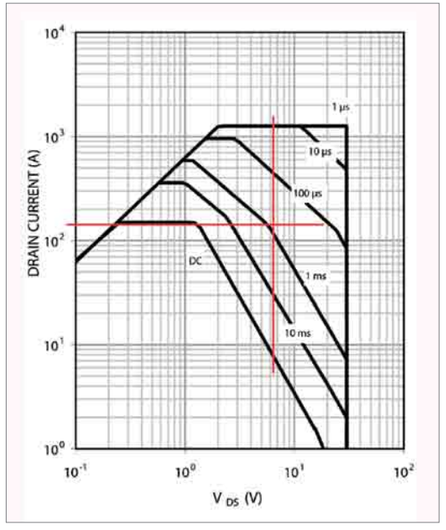



*Figure 6*

MOSFET, and intersect 6.3V with 135A, we get approximately 0.8ms. See Figure 6.
It should be noted that some FETs SOA power lines do not always represent a constant power product. This should be checked and if the line is not constant power then more points should be checked. For example, check VMAX of 13.2V against IFLBMIN = 16 A, derated to 40A. In this case the 6.3V SOA is very similar. If there is no specific requirement for the fault filter, its recommended to further reduce this to account for SOA tolerances and inaccuracies. In this case, lets reduce by 50% to 0.4ms.

Summary of the key spec / component selection for this section:
TSOA_MAX = 400µs

**Powerup analysis**
Now that the timer had been selected, we must check to verify that there is sufficient time available to allow the loads caps to complete powerup. This is determined by how long the startup current profile intersects with the current limit... i.e. how long the timer is active during powerup.

During the power-up phase, the controller will usually hit the current limit due to the inrush current demanded by the load capacitance. If the time set by the TIMER pin is insufficient to allow the load capacitors to charge, then the MOSFET will be disabled and system will not power up. We can use the following equation to estimate the powerup time using an average current limit across the foldback system:

$$t_{CHARGE} = \frac{C_{LOAD}\times V_{MAX}}{I_{AVERAGE} - \frac{V_{MAX}}{R_{POWERUP}}}$$
$$= \frac{5000\times 10^{-6}\ \mathrm{F}\times 12.6\ \mathrm{V}}{33\ \mathrm{A} - \frac{12.6}{10}}$$
$$\approx 1.98ms$$

As the time required exceeds the determined SOA limits, the system would not complete powerup into this size load capacitance. To overcome this the inrush current needs to be lowered to a level below the hotswap control limit at powerup. This is achieved by increasing the effective gate capacitance resulting in a slower powerup time and a lower inrush current. In this way the inrush is controlled using an open loop source follower system. To avoid exceeding the current limit(16A), an additional gate capacitor can be determined as follows to provide an inrush of ~10A:

$$C_{GATE} = C_{LOAD}\times\left(\frac{I_{GATE}}{I_{INRUSH}}\right)$$
$$= 5mF\times\left(\frac{25\mu A}{10A}\right)$$
$$\approx 12.5nF$$

The effective CGD of the MOSFETs can be subtracted from this figure. However, to account for tolerances we can round up to 15nF.

**Powerup time can now be calculated as follows:**

$$t_{POWERUP} = \frac{C_{GATE}\times V_{MAX}}{I_{GATE}}$$
$$= \frac{15\mathrm{nF}\times 12.6\ \mathrm{V}}{25\mu A}$$
$$\approx 7.5ms$$

Summary of the key spec / component selection for this section:
CGATE = 15nF
TPOWERUP =~ 7.5ms

**Timer Capacitor**
Now that the MOSFETs SOA requirements have been determined, and powerup time is satisfied, a TIMER capacitor value can be calculated. This can be calculated as follows:

$$C_{TIMER} = \frac{t_{TIMER} \times I_{TIMER}}{V_{TIMER}}$$

Where ITIMER = 60 µA and VTIMER = 1.0 V,

$$C_{TIMER} = \frac{\left(400 \times 10^{-6}\ \text{s}\right) \times \left(60 \times 10^{-6}\ \text{A}\right)}{1.0\ \text{V}}$$

**Power in MOSFET at startup**
Now, as a final step we need to check that the power being dissipated in the FETs at startup is within the SOA limits of the MOSFET. We can calculate the Energy required to charge the load capacitor as follows:

$$E_{CL} = \frac{CV^2}{2}$$
$$= \frac{5000 \times 10^{-6} \times (12.6)^2}{2}$$
$$\approx 0.397\ joules$$

The power can be determined using:

$$P_{FET} = \frac{E}{t}$$
$$= \frac{0.397}{7.5 \times 10^{-3}}$$
$$\approx 53W$$

(where t = 7.5ms)

Derate this to 133W. Now calculate the current at average Vds (VINMAX / 2):

$$I = \frac{P}{V} = \frac{133}{6.3} = 21.11A$$

Now if we examine the SOA again, we can see that 6.3V and 22A corresponds to >10ms, satisfying SOA limitations.

**Design Complete!**

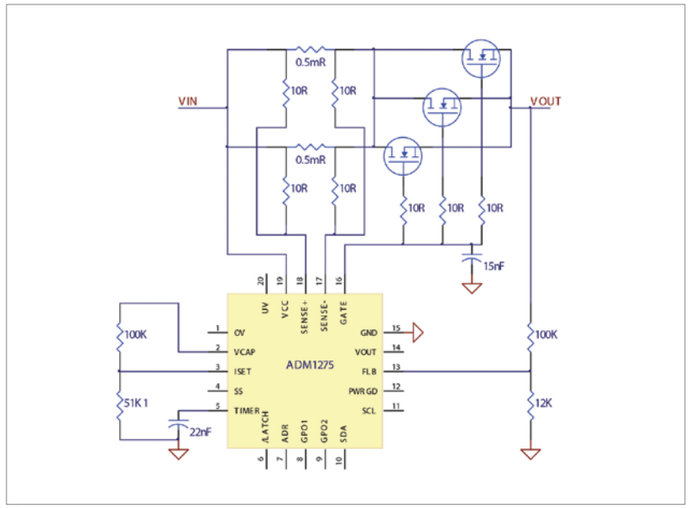


*Figure 7*

Here in Figure 7 is the complete design for the main circuit components.

*Author: Marcus O'Sullivan*
*Applications engineer, Power Management Group*
*Analog Devices*

www.analog.com







# DIGITAL POL IMPROVES KEY METRICS

## Current-sharing second-generation advantages

By Patrick Le Fèvre

Digital power conversion has moved on from being a novelty to widespread acceptance. Ericsson launched its BMR453 quarter-brick intermediate-bus converter in 2008 and followed with an eighth-brick version together with a pair of point-of-load regulators (POLs). Each of these 3E family devices introduced electrical specifications and features remain best-in-class.

The key metrics in power engineers' thinking -whether in consumer appliances or datacenters- are conversion efficiency, power density, and electrical performance. Balancing these elements alongside other considerations—such as feature sets and cost—requires multiple compromises. For instance, because passive components dictate any conventional analogue converter's loop dynamics, designers set the operational "sweet spot" at 50 – 70% of the converter's output potential, as this is where users have previously applied such products.

By implementing a digital control architecture that adapts to line and load conditions in real time, the first-generation BMR450 extends conversion efficiency particularly under light loads, where losses predominate. The digital converter employs adaptive dead-time control for its synchronous buck converter's switches, which safely minimises the period between the MOSFETs being off—during which time currents flow through the devices' lossy body diodes.
The strategy enhances efficiency at operational extremes and helps to flatten the efficiency curve. The BMR463 adds programmable strategies to optimise efficiency under light loads by minimising the effective switching frequency and preventing energy-sapping negative current flow through the lower MOSFET switch. Other new features reflect improvements to the underlying silicon together with proprietary firmware developments. Importantly, the new converter is specified for 4.5 – 14 VDC input and 0.6 – 3.3 VDC output levels to satisfy the wider range of conditions that today's applications demand. Figure 1 shows performance for the conventional 12 VDC intermediate-bus rail and a nominal 5 VDC input level,

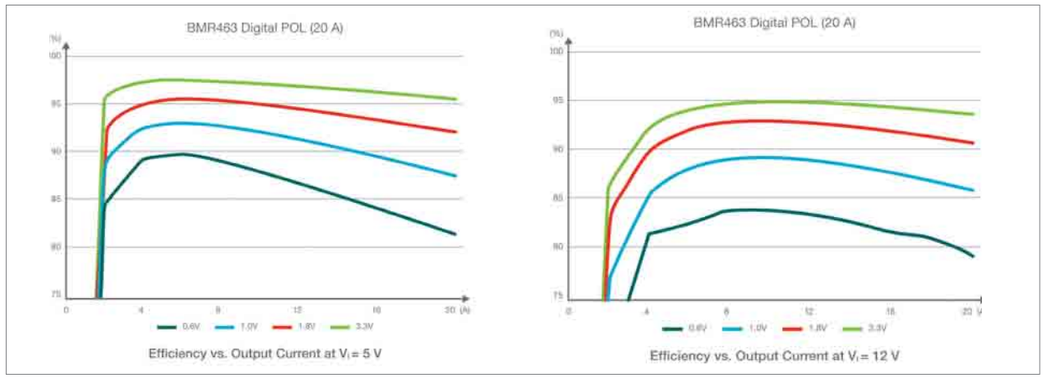



*Figure 1: The BMR463 extends the operational envelope to accommodate 4.5 – 14VDC input and 0.6 – 3.3VDC output levels.*

reflecting the trend towards lower bus voltages due to their potential for optimising system conversion efficiency.

**Digital core delivers dramatic power-density and functionality improvements**

Better efficiency and digital control's greater integration permit a step-function improvement in power density, as figure 2 illustrates for the BMR450 and its analogue PMH8918L predecessor:

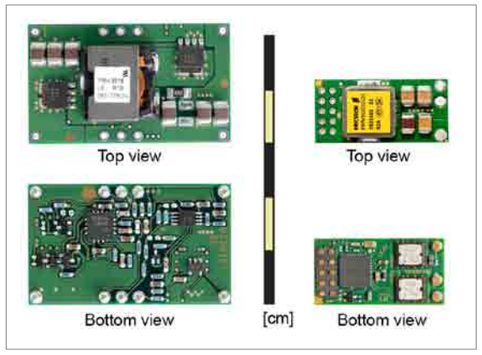



*Figure 2: The first-generation digital BMR450 (right) squeezes 20A from a compact outline that improves power density from the analogue converter's 7.4W/cm3 to 24.3W/cm3*

Apart from tripling power density, the BMR450 integrates a supervisory measurement and control subsystem that the device's PMBus interface makes accessible—massively shrinking circuit-board complexity and area compared with any conventional analogue architecture. Board power management logic can interrogate any 3E family device to read parameters such as output voltage, current, and converter temperature, and can program the device in a running system.

The BMR463 adds a "snapshot" mode that reads key operating parameters and stores them to nonvolatile memory during normal operation, and that can be set to operate automatically under fault conditions. Designing sophisticated PMBus systems is now easier than ever and the potential benefits are huge—ranging from dynamic system optimisation that can drive down energy consumption to data acquisition that enables root-cause and predictive failure analysis.

**Transient response complements basic electrical performance**

The BMR463's electrical performance is typically better than analogue converters of similar power levels. Line and load regulation remain within 3mV at any setting, while output voltage accuracy including temperature effects over the -30 to +85°C operating range is within ±1%. Output ripple and noise vary from 20mV peak-to-peak at 0.6V outputs to 60mV at 3.3V and can be optimised for specific applications by adjusting the converter's default 320kHz switching frequency from 200 – 640kHz.

In the event of a fast output current step, the digital core's nonlinear response loop bypasses the main control loop, increasing the converter's gain-bandwidth product to speed transient response beyond the capabilities of a linear loop. Unlike any conventional analogue POL, it is possible to fine-tune the digital loop's default dynamic characteristics to optimise transient response performance for specific line, load, and output capacitance conditions.

**Standalone and PMBus application versatility**

Like all 3E family devices, the nonvolatile memory that stores the BMR463's setup parameters can be programmed during initial manufacture or later—such as once during a host board's ATE functional tests, or arbitrarily during system operation—to set its output voltage and other parameters via its PMBus interface. The device's "set-&-forget" capability is useful for implementing the power-rail sequencing that multi-rail logic devices require, as well as any slew rate limiting that may be necessary to minimise power transients at system power-up. Also capable of operating in standalone mode for replacing analogue converters, the BMR463's communications header includes pins that support remote voltage sensing, together with a pinstrap that allows one resistor to set the device's output voltage between 0.6 – 3.3 VDC in 28 increments.

At 25.65 x 13.8 x 8.2mm—0.9mm wider than the BMR450—the BMR463 adds two pins that extend its versatility. A group communications bus (GCB) pin allows multiple BMR463s to communicate autonomously. One application is to allow appropriately-configured devices to implement fault spreading, such that a temporary fault in any one converter initiates a predetermined shutdown and restart sequence that protects sensitive multi-rail chips; another is to sequence the application of voltage rails in multi-rail environments during routine power up/down events. Also simplifying multi-rail applications, an analogue voltage-tracking input complements the normal voltage sequencing so the device can track an external reference voltage and ramp its output at the same rate, or at a percentage of that rate.

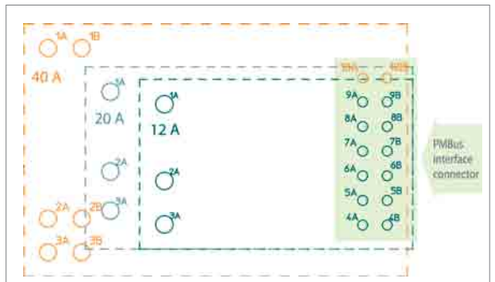
The BMR463's clock synchronisation adds the ability to shift phase angle between devices switching in up to 16 increments, reducing instantaneous loading on the input supply as current peaks are spread out across a whole switching period. The converter now includes a dedicated power-good signal that signifies when the output is within -10/+15% of its target value; these default limits are configurable.

**Autonomous current sharing without OR-ing diodes**

The BMR463 introduces a current-sharing mode that allows up to eight device outputs to be connected in parallel without any OR-ing diodes or MOSFETs to deliver up to 160A. This benefits systems that dynamically power down circuit blocks to minimise static power consumption, such as in response to network traffic patterns in communications systems.

When configured as a current-sharing group, the BMR463 with the lowest position within the group automatically acts as a reference that continuously broadcasts its inductor current via the GCB. Other group members assess this information and adjust their output voltages to maintain equal current delivery between each device. Some artificial droop resistance in each device's output voltage path enables automatic compensation for inequalities such as differing circuit-board resistance paths.

Group members can autonomously set up switching phase differences between them that minimises input-rail stresses and divides the output ripple level by the number of devices in the group. In addition, a current-sharing group is able to dynamically add or shed phases in response to load conditions. This can save conversion switching energy under light loads when fewer BMR463s are necessary to service the output current demand. A group can also provide redundancy, dropping faulty




| Pin | Designation | Function |
|---|---|---|
| 1A, B* | Vin | Input voltage |
| 2A, B* | GND | Power ground |
| 3A, B* | Vout | Output voltage |
| 4A | Vtrk | Voltage tracking input |
| 4B | SGND | Pin-strap ground reference |
| 5A | +S | Positive sense |
| 5B | –S | Negative sense |
| 6A | SA0 | PMBus address pin-strap |
| 6B | GCB | Group communication bus |
| 7A | SCL | PMBus clock |
| 7B | SDA | PMBus data |
| 8A | Vset | Output voltage pin-strap |
| 8B | SYNC | Synchronization I/O |
| 9A | SALERT | PMBus alert |
| 9B | CTRL | PMBus control (Remote Control) |
| 10A* | PG* | Power Good |
| 10B* | SA1* | PMBus address pin-strap |

*only on BMR464

*Figure 3: A common footprint can accommodate 12, 20, and 40A BMR46x family devices.*

phases and switching in replacements—when the group will self-configure to maintain normal operation if it can supply the necessary load current.

**Footprint and packaging practicalities**

Ericsson's designers have evolved a footprint for the BMR463 that makes provision for upcoming BMR46x devices that will extend the output current levels to include 12, 20, and 40A. Figure 3 shows this approach. Board designers can use a uniform footprint to accommodate power level changes when implementing system upgrades. Each BMR46x is available in through-hole or surface-mount versions, and designed to ease automated assembly using standard board manufacturing processes.

An evaluation kit is available that provides a PC-based development environment to explore PMBus applications built around 3E family devices.

*Author: Patrick Le Fèvre*
*Marketing & Communication Director*
*Ericsson Power Modules*

For further application information on digital power conversion, please navigate to

www.ericsson.com/powermodules



# SMD CUBE SKRINKS FOOTPRINT

## Much-improved 1W isolated DC/DC converter

By Ann-Marie Bayliss

With their ability to drastically simplify provision of low-power isolated power rails that are commonly required in applications such as process control and industrial communications interfaces, encapsulated though-hole DC/DC converters became immensely popular following their introduction more than two decades ago.


Designing a tiny DC/DC converter that meets contemporary performance expectations and that provides a degree of future-proofing is not straightforward. The first challenge is to select a topology that meets the size constraints that miniaturisation demands, yet is capable of adequate output power delivery, isolation and regulation. The chosen approach should be able to address a range of common input and output voltages as well as ideally being extensible to deliver more power from a similar platform. The need for an isolation barrier that withstands typically 1 kVDC implies transformer coupling that requires ac primary drive and secondary rectification whose implementation inevitably involves compromises that mainly lie between component count and conversion efficiency.

The conventional minimum component count approach uses a saturating 'Royer' circuit, a self-oscillating push-pull topology, in which a pair of bipolar transistors drive antiphase primary transformer windings and derive their base currents from opposite ends of a centre-tapped auxiliary winding. Applying a dc input voltage through a start-up bias circuit turns on one transistor, which remains on until the transformer's core saturates, the transistor gain-limits and all transformer winding voltages collapse. Residual energy in the transformer causes reversal of the polarity of winding voltages which switches off the first transistor and biases the second to the 'on' condition which then starts to drive its winding to saturation. The process repeats to sustain oscillation at a frequency that is proportional to the input voltage, creating a square-wave output voltage for rectification.

This basic circuit has several limitations, notably its lack of active regulation—the output voltage is a function of the input

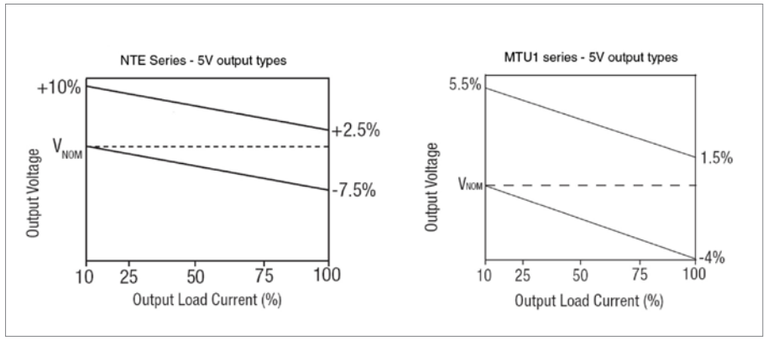



*Figure 1: The MTU1 series significantly improves output load regulation performance.*

voltage, internal losses and the transformer's turns ratio—together with poor efficiency due to semiconductor switching and core magnetic losses at the high frequencies that miniature transformers require. Well-known variations around the theme include modifying the circuit to avoid lossy core saturation by using a second drive transformer which has potentially higher efficiency but at the cost of complexity and size.

**Electrical specification enhancements**

By combining proprietary circuit enhancements and recent component fabrication techniques, designers can improve the load regulation of such a converter. For example, Murata Power Solutions' engineers were able to increase their MTU1 part's load regulation performance to a maximum -4, +5.5% from 10% of full load upwards. By comparison, previous ranges achieved -7.5, +10% see figure 1. For many applications, the load regulation these enhancements offer obviates the need for inefficient and space-hungry linear post-regulation stages.

At the same time, a major improvement to the part's toroidal magnetics helps to improve efficiency to the range of 83 – 88%. Also, the switching frequency has reduced from nominally 110 kHz to 82 kHz for 5V-input MTU1 parts and 90 kHz for its 12V-input variants. These steps likewise contribute towards lower dynamic losses. Notably—and as figure 2 shows—the efficiency curves reach or exceed 80% at around 40% of output power capability and are virtually flat from 50% upwards. These efficiency improvements translate into an approximately 56% reduction in internal power dissipation that reduces internal hot-spots maximising reliability while minimising the heat load that the host equipment has to accommodate. The MTU1 series requires no derating over its -40 to +85°C operating range. Other electrical specification enhancements include reduction to reflected ripple current from around 30 mA peak-to-peak to 5 – 6 mA and isolation capacitance reduction of between two and three times. These attributes greatly ease input filtering needs. The reduced capacitance further isolates input and output, making the part far less susceptible to transmitting noise through its isolation barrier which could potentially disturb sensitive loads.

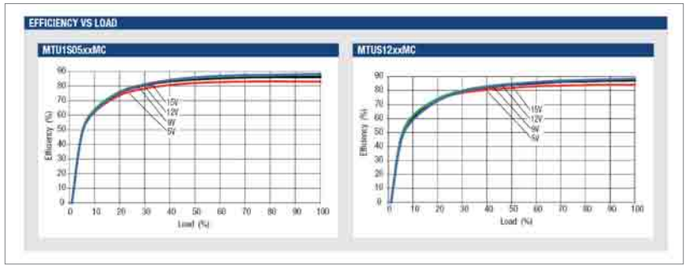



*Figure 2: The MTU1 series meets or exceeds 80% efficiency from ~40% of its output power capability upwards.*

**Design for manufacture achieves MSL1**

Significantly—and unlike some plastic-encapsulated packages that industry-standard components employ—the MTU1's composite assembly has a level 1 rating for moisture sensitivity (MSL1).

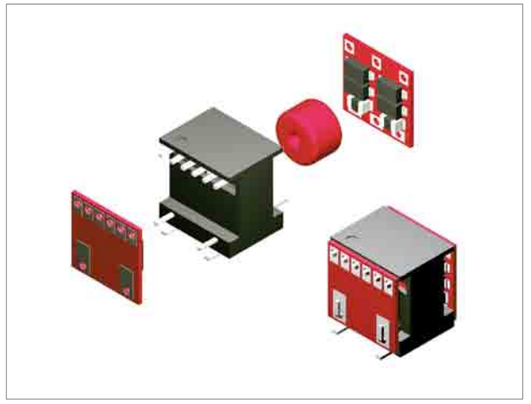


*Figure 3: The MTU1's cube-like package achieves MSL1 and eases automated assembly.*

Moisture absorption and retention is a major issue for many surface-mount devices as it can generate large stresses when the part is subjected to a rapid and very large temperature rise, such as during lead-free reflow processing that can reach peak temperatures as high as 245°C. The resulting outgassing can easily destroy the device and is generically known as "popcorn cracking".

As a result, component manufacturers classify the moisture sensitivity of their parts on a scale that IPC/JEDEC J-STD-20 rates from 1 through 6, where an MSL1 rating signifies that the part is immune to popcorn cracking regardless of its exposure to moisture. The MTU1's package design dispenses with the pre-baking procedures that many parts rated less than MSL1 routinely require and that can negatively impact upon their solderability. Additionally, for MSL1 rating, no expensive handling and storage precautions are necessary. Furthermore, the MTU1's open-frame construction is designed to reflow safely during processing and negate any tendency towards internal solder bridging, while the cube shape's flat top surface makes it easy for standard vacuum pick-&-place nozzles to manipulate.

*Author: Ann-Marie Bayliss*
*Product Marketing Manager*
*Murata Power Solutions*
www.murata-ps.com

# DIRECT FUEL INJECTION

## Implications for automotive MOSFET devices

By Don Zaremba

There is a pressing need within the automotive industry for realizing greater degrees of fuel economy. This is being driven by rising oil prices through ongoing political uncertainty in many oil producing countries.

There are growing difficulties in extracting remaining oil reserves and increased sales within emerging markets such as China, Russia, Brazil and India married with intensifying environment concerns. In an attempt to stem pollution levels, the US Environmental Protection Agency (EPA) has set guidelines that from 2012 onwards fleet-wide greenhouse gas emissions should be cut by 5% each year. At the same time car manufacturers still need to meet customer expectations in terms of performance, so that they can keep ahead of their competitors. This is certain to put a great deal of pressure onto manufacturers' engineering teams, and will call for more innovative solutions that can tackle these disparate demands. Maximizing the effectiveness of every drop of fuel is something that no car maker can now afford to ignore.

One way that fuel efficiency can be improved is to make enhancements to the fuel delivery mechanisms being utilized. The following article will look at how the latest car models will be able to achieve this goal and describe the supporting electronics involved.

**Modern fuel delivery systems**

Modern engine designs are now starting to employ direct-injection. Here fuel is introduced straight into the cylinder rather than being premixed outside. This technique has major advantages as it allows more accurate control of the quantity of fuel used and the injection timing, leading to an increase in the vehicle's horsepower combined with a lower fuel intake. As a result of implementing direct-injection, car manufacturers will be able to meet government guidelines for reducing vehicle emission levels while still producing the high performance cars customers want.

However direct-injection calls for even more sophisticated control electronics and puts exacting demands on the components being utilized.

Traditionally electronic fuel injection would be carried out via a solenoid-based injector. This method has proved to be both inexpensive and highly reliable. As a result it still sees widespread use today. Unfortunately it is also relatively inefficient. There is a growing trend toward the implementation of piezoelectric injectors - with fine, rapid, multiple injections allowing the greater fuel delivery control desired, but they can prove expensive and require high voltages to activate. The car market has become increasingly competitive in recent years, with manufacturers seeing their margins tightened. Reconciling the increased cost of more advanced electronics for fuel delivery is difficult. Today's car owners will not pay more for improved performance, they expect that already. Automotive electronics has become similar to computing and portable electronics sectors in that regard – with ever increasing functionality and performance being met by lower and lower price tags.

**The role of power MOSFETs in modern fuel delivery systems**

Power MOSFETs are normally used in fuel delivery to switch the injector on/off per commands from the ECU (Engine Control Unit). One MOSFET will be employed for each injector. As fuel delivery systems have evolved, so have the MOSFET's requirements. This has meant that semiconductor companies have been forced to develop new generations of devices that have enhanced performance in a number of key metrics.

1. Operating voltage – some MOSFET parameters for direct-injection will be notably higher than for standard injection systems. Direct-injection systems generally require higher pull-in current (in order to get the solenoid operating against high cylinder pressure). This high current must happen quickly (due to limited time available to inject fuel in the engine cycle, which decreases as the RPM rises), therefore a higher voltage rail is required. Direct-injection systems can have rail voltages >100 V (as opposed to around 50 V for standard injection systems). Thus higher voltage MOSFETs need to be specified, along with voltage boost power supply circuits. Piezoelectric injectors also require high voltages to be activated, typically 200 V or above. In general, there is a lack of auto-qualified MOSFETs for high/medium voltages. As piezo applications increase, module suppliers will demand a larger selection of suppliers from which to buy the required MOSFETs.

2. Operating current - Higher currents call for lower On resistance (Rdson) devices to meet module voltage drop requirements and to reduce power dissipation in the module. Newer systems are considering trench technology (as opposed to established planar process technology) in order to reduce overall system cost. Current trench technologies can reduce active die area of a planar device with equivalent Rdson by 50%.

3. Switching speeds and repetitive UIS - The timing for an engine, even running at 10,000 RPM is not that fast in electronics terms, considering that other applications, like CPU VRM switches, run at hundreds of KHz, for example. Nevertheless increasingly complex fuel delivery algorithms are causing device switching speeds to become a more important factor. This is because the modern systems we have discussed are now injecting fuel in multiple separate bursts, instead of a single burst. The difficulty in multi-injection systems is having enough time to ramp the current again and again. If timing is not critical, the circuit designer can clamp the inductor voltage with a diode to the supply rail, thus not putting the MOSFET switch into avalanche mode at each turn-off cycle. However with increasing injections, designers often have no choice but to allow the MOSFET switch to flyback, affording maximum voltage across the solenoid inductor. This requires MOSFETs with strong UIS (Unclamped Inductive Switching) capabilities. Considering a MOSFET could see >1 billion injection cycles in a vehicle's lifetime, the repetitive UIS capability of the specified MOSFET is of great importance to system designers. As yet, however, the repetitive UIS capability of MOSFETs is not a well characterized parameter across the various vendors on the market. Efforts are now in progress to better understand reliability concerns, especially comparing new trench technologies to existing planar technologies. Trench MOSFET technology is often perceived as weak with

regard to UIS capability, when compared to planar MOSFET technology. One reason for this perception is a trench device with equivalent Rdson to a planar device has significantly less active die area. For a properly designed and manufactured MOSFET, UIS capability is a function of thermal capability, so a trench device will always exhibit lower UIS capability than a planar device which is equivalently Rdson rated. The geometry of the trench structure results in a more serious concern however. In high current avalanche operation, trench technology affords hot carrier injection into the gate oxide, which can result in shifted DC parameters over multiple avalanche events. These parameter shifts can be minor, but DC parameter behavior does need to be better understood over hundred of million to billions of avalanche events.

4. Thermal considerations - Powertrain electronics are typically housed within the ECU. The ECU's ambient temperature requirements are usually the most uncompromising in the vehicle, spanning from -40 C to 125 C or above. This means that MOSFETs with higher operating temperature specifications must be designed in, capable of dealing with broader temperature ranges. To compound problems further, advances in fuel delivery systems (with new circuit topologies requiring high side switching, boost supply, and sometimes to switch down to the battery rail for hold current) have led to larger numbers of MOSFETs being incorporated into the ECU, heightening the power density. The board sizes of ECUs never increase due to the cost implications, as it would call for retooling and prevent cross-utilization of the same electronics hardware across multiple car models. This fact is driving the industry to introduce smaller, more thermally efficient MOSFET packaging. Packages have changed from TO-220, to D2PAK, to DPAK, to the newer, more compact SO8FL options. But the smaller packages, and smaller semiconductor dies drive operating temperatures up - once again leading to reliability concerns resurfacing, especially in the case of repetitive UIS (note that peak power in avalanche during an injection can be measured in kW).

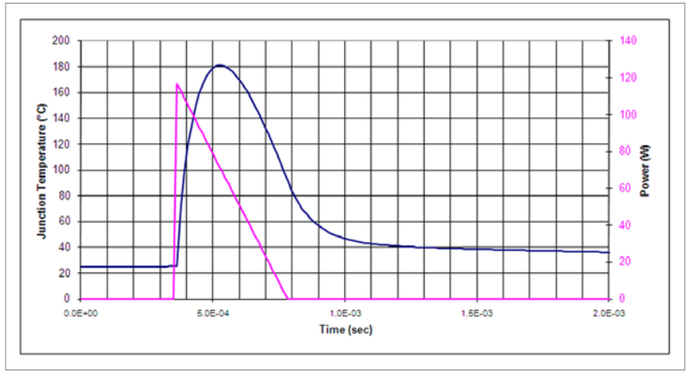



*Figure 1: Estimated junction temperature rise for a given power pulse assuming an inductive load*

Any question about the reliability of a car model can lead to dire consequences. It may result in expensive recalls being carried out and have huge impact on the manufacturer's branding. As a result, sourcing power components which have the high level specifications needed is vital.

The introduction of high performance devices such as the ON Semiconductor NTD6415ANL N-channel planar based power MOSFET will allow car manufacturers to support more advanced fuel injection techniques while still assuring long term vehicle reliability and raising performance levels. This device is AEC-Q101 qualified so that it can deal with tough automotive environments. It has an Rdson of only 52 mΩ at 10 V and supports

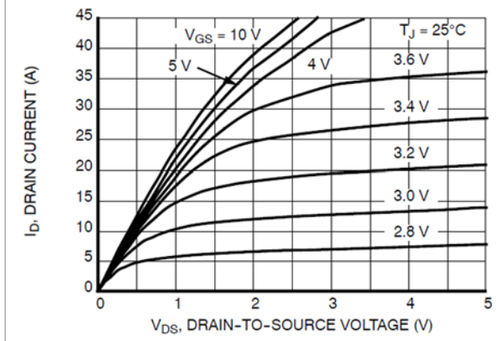



*Figure 2: On-region characteristics for NTD6415ANL*

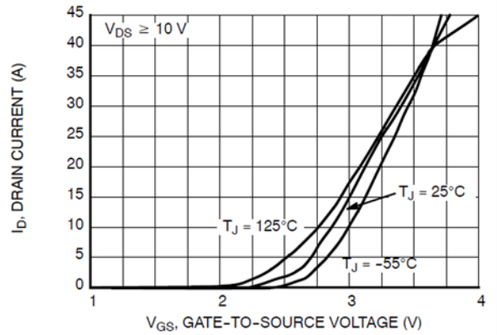



*Figure 3: Transfer characteristics for NTD6415ANL*

voltage levels of 100 V and currents of 23 A. Offered in a DPAK package its operating temperature range covers -55 C to +175 C, allowing the extreme heat levels found in direct-injection systems to be dealt with. Likewise, its thermal resistance characteristics (1.8 C/W junction-to-case) allow rapid heat dissipation and safeguard against faults arising. The company is also currently developing trench-based MOSFET devices to address this application area.

In summary, migration from multi-port injection to direct-injection into the cylinder will markedly improve the effectiveness of fuel delivery systems for gasoline engines. Direct-injection is far more efficient than traditional injection techniques, raising performance levels while requiring less fuel. It affords greater precision of fuel delivery, thus reducing emissions and improving fuel economy. Proliferation of direct-injection throughout the automotive industry will have a huge benefit to the long term protection of the environment.

Advances in power semiconductor technologies are allowing manufacturers to simultaneously meet consumer demands for improved vehicle performance, while gaining higher fuel efficiency and lowering the impact from exhaust emissions. The new breed of MOSFETs being brought to the market by forward thinking manufacturers with specialist knowledge of the automotive sector are able to cope with the high voltages and extreme temperatures required by direct-injection systems.

*Author: Don Zaremba, Applications Engineer,*
*MOSFET Business Unit,*
*ON Semiconductor*
www.onsemi.com

# PAIN MANAGEMENT IN POWER OPTIMIZATION

## Best practices for reducing power, improving productivity and delivering SoCs on time and on budget

By Cary Chin

Power has always been an integral part of consumer electronics, but increasingly we can do more things with a single device. That trend, above all others, has moved power consumption from an afterthought to a critical part of the architecture of the processor, the SoC and even the end device itself.

For SoC architects and engineers at all levels of the design flow, the tradeoffs between area, power and performance are now unevenly weighted toward power. And while there are numerous tools on the designer's belt to solve these problems, the burden each of those places on the verification side of the process has become overwhelming.

All of this can mount up very fast in terms of cost, both in non-recurring engineering hours and re-spins after initial tapeout, which at advanced nodes can easily run into the tens of millions of dollars. But even those costs pale in comparison to the cost of a missed market window.

**Architecting a good plan**

Every SoC requires lots of up-front planning. The better the plan up front, backed up by previous experience, the less pain when it comes to verifying that everything works.

Creating a good plan requires a learning curve at 45nm and beyond because there are simply too many gates and wires and too many interactions across multiple power islands to use the old methods of doing things. High-level models need to be created to be able to spot inconsistencies up front, whether that includes high-level synthesis for the RTL, software prototyping models or power modelling in the architecture. At 45nm and beyond, each one of these techniques speeds up the design process. Below 28nm, it's virtually impossible to create a chip in a reasonable market window without them.

Using those models, architects need to map the future functionality of an SoC. What is the first chip that will be derived from a model and what will the last derivative look like? Will the functionality be built into software or hardware? Will the intellectual property blocks come from multiple vendors and do those blocks work at the same voltages?

Moreover, what are the marketing goals for the chip? What is the minimum performance and the maximum power usage? Will battery life be a competitive issue? How many functions will be combined onto the chip versus another chip in a package?

Perhaps even more troublesome is the testing of the IP blocks and the models themselves. From the from the architecture of the block to the environment in which it is used, low power operating modes and conditions are notoriously difficult to reproduce and test. And with packaging now considered an important aspect of the overall design, particularly when it comes to power dissipation, the problem becomes even more complex.

In fact, the only place where some of the complexity has been taken out of the design is in the layout. Restrictive design rules imposed by foundries for the majority of their customers at 32nm and 28nm is a way of making sure that when a chip gets designed, it can actually achieve reasonable yields. These are business driven rules so the foundries can successfully build chips. But even in this case, Design Rules Checking complexity is way up, and new problems due to extremely small geometries are being introduced. Design for manufacturing suites can help refine the layout even further and offer a number of tradeoffs in terms of what happens when polygons are drawn one way versus another on a piece of silicon.

Increasingly, however, even those tradeoffs are no longer just performance and area-based. The parasitics of the interconnects on a chip have become incredibly complicated. Power, both static and dynamic, needs to be taken into account throughout. So does the ability to manage those tradeoffs. In the past, if this was done at all, it was typically done by hand. There are now tools to make this all work.

None of this can be done purely statically anymore. The impact on I/O and timing can be modeled statically, but they need to be tested dynamically—and usually with at least a prototype of the software that will be running on the hardware once it is developed. And if the entire team wants to succeed, they now have to start having conversations up front with the people who will be testing and verifying the entire system.

A novel approach to managing the pain in chip design is using "in-design technology," a concept that is fast becoming much more important at advanced technology nodes. Rather than just developing the pieces—circuits, blocks, etc.—through individual steps in the flow, analysis technology is shared at each step. For engineers used to working with individual point tools rather than a suite of tools, this is something of a change. While individual tools can be used, the bigger picture needs to drive them and take priority in order to ensure the best optimization and smooth signoff.

That's why it's absolutely vital at the most advanced geometries to use the most integrated tools available at each step of the design process rather than just point tools that do a specific task without understanding the other parts of the process. At advanced nodes the requirement for integration of tools that understand power can mean the difference between hitting a power budget and creating a very costly mistake.

Synopsys IC Compiler uses in-design technology to leverage the analysis engines of Primetime® for timing analysis, PrimeRail for power rail analysis, and IC Validator for physical verification during

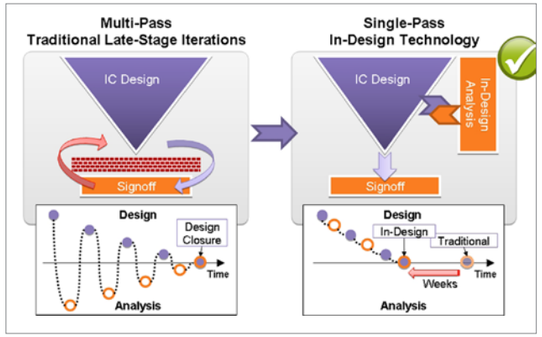



*Figure 1: Benefit of In-Design Technology in IC Design*

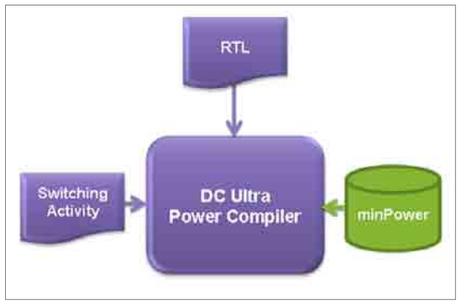



*Figure 2: DesignWare minPower Components enable datapath optimization based on architecture and topology, and data encoding and gating*

the physical implementation process to identify and avoid potential problems, and accelerate overall time-to-tapeout.

At a much higher level, Synopsys DesignWare® minPower Components allow DC Ultra with Power Compiler™ to use power-costing as the basis for high-level datapath architectural choices.

These are examples of integrated technology for power management and optimization within the Galaxy™ Implementation Platform. Similarly, within the Discovery™ Verification Platform, VCS® with MVSIM performs voltage level-aware simulation with an understanding of voltage values to ensure correct operation of complex low-power designs.

**Getting the team to work together**

There's a big difference between the way hardware and software engineers approach problems, and that difference is magnified the further up the software stack you move.

That means both teams have to work together and be in sync throughout the development of the chip. A change on one side has to be reflected on the other, and it has to be reflected in all the models that have been created, whether they're for power, hardware blocks, transactors or software—including prototypes of software that will run on the hardware. In the power realm, a change in the hardware can affect how efficiently the software utilizes that hardware. The corollary is also true, where a change in software can impact the power efficiency of the hardware.

For example, an RTOS that does exactly what a specific size core or processor needs can use significantly less power than a Linux operating system on a general-sized core. Likewise, a powerful multicore processor running a single-threaded software application or kernel is no faster than a single-core processor running the same software.

But this kind of synchronizing of hardware and software teams can only be achieved with buy-in from upper management and choosing tools that can work together.

Companies that have begun to deploy these kinds of bridges report success in churning out chips at the most advanced process nodes on time and on budget, normally using engineers that can bridge the gap between the hardware and software engineers. They basically work as translators back and forth between the teams as they move down the line toward tapeout.

**Verifying it all works**

Final verification of a complex SoC has certainly become a daunting task. But assuming all the necessary steps were taken up front, that pain can be eased substantially. IP can be verified even before it is used in a design. Pre-existing blocks can be verified. And models can be verified in advance.

What cannot be fully verified are the interactions between aspects of the chip and all the variables that go along with them. Consider the smartphone example. A person is listening to music when a call comes in. Does the music power down and then power up when the call is finished, or does it remain on in the background? And if it does stay on, how does that affect the thermal budget?

With these complexities understood and the right tools and support put in place right from the start, projects with power as a key differentiator, need not be so painful.

*Author: Cary Chin*
*Director of Technical Marketing*
*Synopsys*
www.synopsys.com





# INCREASING EFFICIENCY

## Best-in-class value IPM-Based drive designs

By Mark Steinmetz

The Intelligent Power Module, IPM, has been a mainstay in motor speed control designs. And with good reason: Such designs are relatively easy and cheap to implement. With onboard gate drivers, protection, and a six pack IGBT array integrated, it takes very little engineering effort to quickly develop an effective design. Utilizing a stamped lead frame, plastic package, and high-volume components, and given an automated production line, the IPM has all the ingredients necessary to manufacture a low-cost component solution.

However, standard IPMs are not the panacea they would seem to be. Lacking a front end converter - that is, a diode bridge array - and a PFC boost converter section, they fall far short of the mark for highly efficient, IPM-based drive designs. Vincotech has a new IPM module platform that incorporates all these sections - the flowIPM-1B. It is a complete single-component solution.

Housed in Vincotech's ruggedized, low inductance, flowPIM-1 package, the flowIPM-1B meets the application needs of harsh industrial environments.

**Architecture**

Figure 1 shows the schematic of the flowIPM-1B. It depicts a complete drive solution featuring a full bridge diode converter, single boost PFC with driver and boost diode, six-pack IGBT stage with driver, shunt resistors, and thermistor.
The flowPIM-1B offers considerable value and great benefits for low-power drive applications:

- Highly efficient, IPM-based drive design with converter and PFC included
- No external point-to-point connections for switching elements) and low-inductance

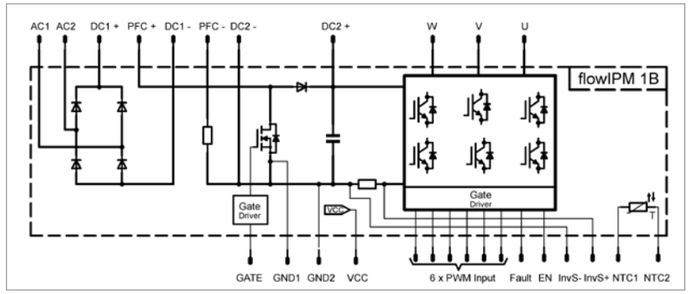



*Figure 1: Schematic of the flowIPM-1B*

module design, resulting in far less EMC/EMI than with a discrete solution
- Compact integrated module solution – small footprint that takes very little PCB real estate
- Highly reliable with no interconnections necessary between components
- 100% factory tested
- Reduced time to market with less time devoted to design and testing

**Performance**

Responding to customers' demands and insights gleaned from studies of the market for low-power drives, Vincotech now offers a full lineup of modules with various options. The ultra fast boost diode-based P953A and SiC boost diode-based P953-A10 both contain a 600V/4A/350mΩ PFC mosfet, utilize a 600V/4A IGBT six-pack, and address up to 1KW drive designs. The ultra fast boost diode-based P955-A and SiC boost diode-based P955-A10 use a 600V/10A/190mΩ mosfet alongside a 600V/10A IGBT six-pack, which increases power handling for up to 2kW designs. The switching components are enhanced with Kelvin emitters for faster switching, resulting in lower losses. In combination with a low-inductance design, these features enable the designer to employ a higher switching frequency, resulting in an application that uses smaller and fewer power components such as inductors, noise filters, and the like.

**Innovative Powerflow Package**

**Design**

Vincotech engineered the flowPIM-1B pin layout specifically to facilitate PCB design. The control signal pins reside together on one side of the module. Power line pins on the opposite side of the module are grouped by functionality to create a power flow structure.


*Figure 2: Power Line and Control Pins reside on opposite sides of the package*

**Why Power Factor?**

Adding power factor to a drive design does increase system cost since it requires a few additional components such as a power inductor and additional switching elements – i.e. mosfet, boost diode. However, this small incremental cost in the drive will save the end user in both installation costs and energy savings.

**Reliability**

In conventional designs, high performance/ high reliability and economy are to some extent mutually exclusive. The designer is compelled to strike a balance between performance and reliability on one side of the scale and cost on the other. Obviously, the designer must factor reliability into the cost equation - the last thing a manufacturer wants are field failures, both long and short term. Modules that use a ceramic substrate solve this problem. This results in a solution that remains reliable over the long term, sparing the manufacturer costly warranty returns. Modules have fewer point-to-point solder connections which increases reliability. A low-cost, unreliable discrete design can adversely affect the manufacturer's credibility.

**Lower Manufacturing Costs**

Many designers choose a discrete solution based solely on the cost of components, which fails to take the total cost of ownership into account.

Discrete cost factors
- Aligning, attaching, and fastening discretes to the heat sink entails manual labor
- Individual electrical isolation material is necessary for each discrete device
- The design mandates individual heat sinks
- Using a single heat sink for discretes requires more holes

To drive down manufacturing costs for designs using discretes, Vincotech offers its new Press Pin technology on the flowIPM-1B and other modules. Modules are simply pressed rather than soldered into the PCB to reduce assembly time and costs.
Press fit pin design is well established in the automotive industry and provides a reliable and gas-tight connection to the PCB. Further advantages of press fit technology include reuse of the PCB and design flexibility. The module can be removed without damaging the PCB, thus allowing for the reuse of the PCB with a new module. Design flexibility is guaranteed by the elimination of the need for soldering; the module can easily be mounted on either side of the PCB at no extra cost or effort.

**Typical Application Example**

In a typical application, today's modern window air conditioner would benefit by increasing its efficiency. These are consumer appliances, so the manufacturer must pay close attention to cost. The implementation of the flowIPM-1B for the compressor motor inverter enables a universal input voltage from 100VAC ~ 240VAC. This allows the manufacturer to select a single motor for a given BTU size (up to 6500 BTUs) to cover the different voltages required in US, European, and other markets. A smaller, lighter, and more efficient motor driven by a variable power inverter replaces the standard compressor motor. Using a single motor for each model size creates economies of scale, thereby further reducing costs. And the higher efficiency rating helps differentiate the manufacturer's product from the competitors'.

**Comparing Costs**

Many engineers balk at the higher cost of modules over an equivalent multiple-component discrete solution. Vincotech has painstakingly qualified the components used within each module and the entire assembly to ensure it meets all datasheet specifications, including minimum, typical, and maximum values. Using a cheaper discrete part with half of the data provided certainly does not make a product more durable. Vincotech's modules are subjected to rigorous battery of specifications and functionality tests for each type of module. A discrete solution is the sum of its many individual parts, which must be tested collectively. Modules, in contrast, take the guesswork out of the topology, making the design more efficient and reliable and reducing test time during the manufacturing process. All this drives down design and manufacturing costs.

**Evaluation Board**

Vincotech has introduced a flowIPM-1B evaluation board to facilitate engineers' evaluation and development efforts:

- P950 power module featuring rectifier, PFC, six-pack with driver, and current sensing shunts
- Complete 1 kW PFC circuit with PFC controller (switching frequency settable by resistor)
- 110 VAC – 230 VAC single phase input with 2 stage EMC filter, fuse and NTC inrush protection
- 380 VDC link (settable by resistor)
- Phase 230 VAC motor output
- V TTL-compatible inverting (active low) PWM inputs for the six-pack
- Dedicated enable input (active high)
- Fault output signal (open collector)
- AC/DC converter for powering the PFC controller, measurement circuit and gate drivers in the module
- PCB designed to satisfy IEC61800-5-1, pollution degree 2, overvoltage category III standards

**Conclusion**

Vincotech's new flowIPM-1B module offers an innovative new way to design a highly efficient, PFC-based IPM with very little effort. The same modules, without PFC (1B06INA004SA – 1kW; 1B06INA010SA – 2kW) are also available. A manufacturer can use a single board design to offer both standard (without PFC) and premium (with PFC) drives. The single streamlined design creates economies of scale and cuts costs. Beyond that, Vincotech offers the press pin option as well as pre-applied phase change material to further reduce manufacturing costs. A full line of module-based solutions with extraordinary reliability and optional press pins and pre-applied phase change material – all this adds up to best-in-class value.

*Author: Mark Steinmetz*
*Field Applications Engineer*
*Vincotech GmbH*
www.vincotech.com

# Special Report: White Goods

PSD EUROPE
Power Systems Design: Empowering Global Innovation

Inside:

# COST COMPETITIVE SiC

## Technology behind the SiC MOSFET and applications

By Bob Callanan

Silicon carbide (SiC) is a compound semiconductor that is superior to silicon (Si) in several respects. These advantages stem from SiC's ~10x higher critical breakdown field, ~2.8x higher thermal conductivity, and ~3x higher bandgap compared to Si. For the future, the compelling cost of ownership over lifetime argument could find these devices in future everyday appliance applications.

The higher critical breakdown field allows for a much thinner device for a given breakdown voltage. This reduces the on-resistance per unit area by as much as two orders of magnitude compared to Si. Conversely, the higher breakdown field of SiC also allows the realization of SiC MOSFETs with voltage ratings up to 10kV. The higher thermal conductivity allows higher current density capability for a given junction temperature. Lastly, the wider bandgap of SiC over Si affords about 1 to 2 orders of magnitude lower leakage current at high temperatures.




*Figures 1 &2: Forward conduction characteristics comparison*

The advantages of the 1.2kV SiC MOSFET technology are best illustrated by a comparison with existing 1.2kV Si switches. The forward conduction characteristics of the SiC MOSFET, along with a Si MOSFET, TFS, and NPT IGBTs are presented in Figures 1 & 2.

At 150°C, the RDS(on) of the SiC MOSFET increases only about 20% from 25°C to 150°C whereas the Si MOSFET device's RDS(on) increases by 250%, as shown in Figure 3. This has a significant effect on system thermal design.

Being a majority carrier device, the SiC MOSFET does not have a minority carrier current tail like the Si IGBT. This results in significantly lower switching losses and allows easy paralleling. The inductive switching loss versus temperature is shown in Figure 4. In all cases, the SiC MOSFET

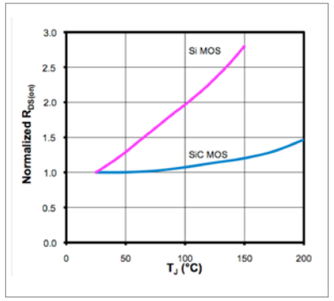



*Figure 3: Normalized RDS(on) vs. temperature*

switching losses are significantly better than its silicon competitors.

In general, the 1.2kV SiC MOSFET can be used in almost any application presently using a 1.2kV Si MOSFET or 1.2kV Si IGBT, where higher efficiency and higher operating frequency are desired. These applications can vary from solar and wind inverters and motor drives to induction heating systems and high voltage DC/DC converters. The application space for the SiC MOSFET is shown in Figure 5.

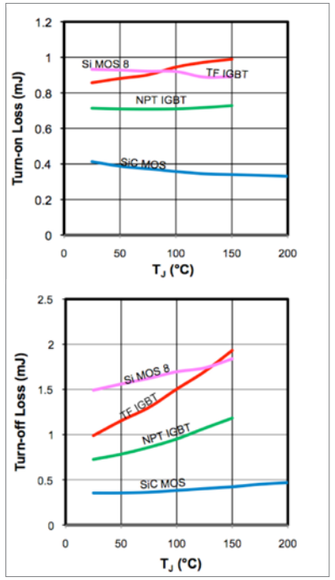



*Figure 4: Switching loss vs. temperature comparison (VDD = VCC = 800V, ID = IC = 20A, RG = 10Ù)*

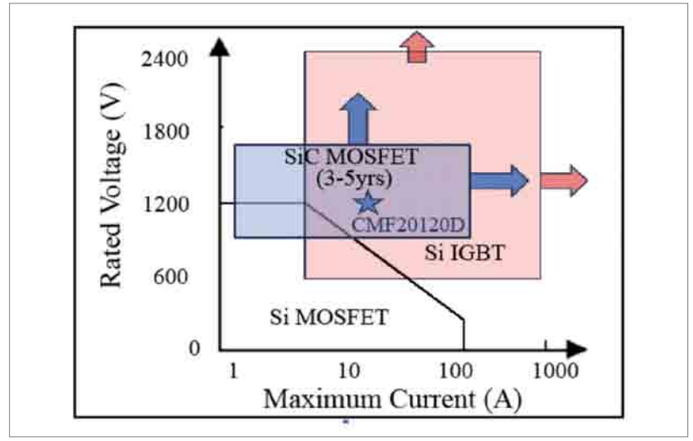



*Figure 5: SiC MOSFET Application Space*

The solar inverter application will illustrate the value proposition of SiC MOSFETs. The comparison vehicle was a 7kW, 16.6kHz three-phase grid connected solar inverter employing a B6 topology developed by the Fraunhofer Institute. This topology uses a split link DC capacitor with a connection of the neutral conductor to the center point of both capacitors. The unit connects to a 400V grid, therefore 1.2kV IGBTs are used for the switching devices. The Si IGBTs were directly replaced with 1.2kV SiC MOSFETs, with no circuit optimization and this resulted in a significant improvement in efficiency as shown in Figure 6.

The SiC MOSFET improved the maximum efficiency by 1.92%, and the overall European efficiency rating improved by 2.36%. This equates to a 50% reduction in overall losses in the system. Furthermore, the heat sink temperature was reduced by 43 °C. Further research has also been conducted with these devices by ISET (Institut fur Solare Energieversorgungstechnik) & SMA GmbH, yielding a 99% maximum efficiency rating in their three-phase grid connected system.

Another application for SiC MOSFETs is motor drives. An experiment was performed at Cree [6] where the Si IGBTs were directly replaced with SiC MOSFETs in a 230VAC 2.2kW three-phase motor drive operating at 16kHz. The SiC MOSFETs demonstrated a 2% efficiency improvement along with a 50% reduction in heat sink temperature. In both the solar inverter and motor drive, the losses are essentially cut in half. This allows

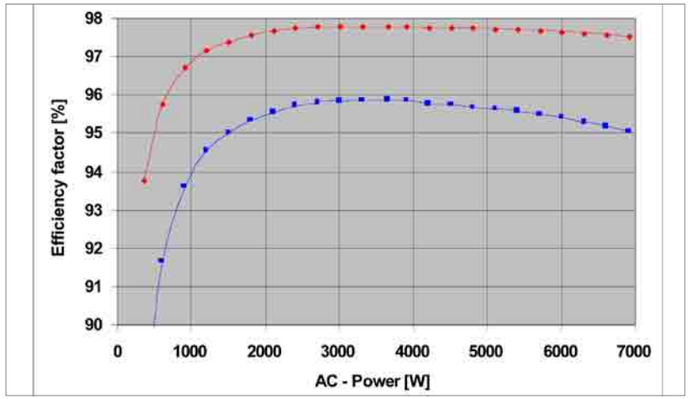



*Figure 6: Comparison of three-phase PV inverter efficiency*

substantial simplification of the cooling systems, such as elimination of fans, etc. Furthermore, higher operating frequencies (48kHz+) are possible, allowing for significant reductions in the size and weight of inductors and EMI filters.

SiC MOSFETs find application in three-phase 480V power factor correction circuits where 1.2kV switching devices are required. The Si MOSFET has excessive conduction loss at this voltage, whereas the Si IGBT has higher switching loss, thus limiting the practical upper operating frequency. The combination of low conduction and switching losses makes the SiC MOSFET ideal for this application, promising higher efficiency and the ability to operate at higher frequencies, thus reducing the size of the inductive components.

High power converters are employed for welders, plasma cutters, and other industrial equipment. The same issues occur for these applications when a 1.2kV switch is required. To efficiently operate Si IGBTs at frequencies above approximately 24kHz, resonant topologies need to be employed involving the use of additional resonant components and usually result in higher transformer RMS currents per unit of output power. An alternative to this is to use a multi-level topology using lower voltage Si MOSFETs, which requires doubling the number of switches. The high frequency capability of SiC MOSFETs allows the use of simple two-level hard switched topologies. A 10kW, 1kV DC-DC converter operating at 32kHz (hard switched) has been demonstrated with over 97% efficiency.

**Summary:**
SiC technology represents a fundamental change in power electronics. The price of a SiC MOSFET is more expensive than a Si MOSFET or Si IGBT. However, the entire system and energy savings potential need to be considered in assessing the overall value proposition that this technology delivers. The following system savings need to be carefully considered:

**Reduction of the cost of passive components**
In many instances, the cost of the passive power components dominate the overall bill of materials cost. Increasing the switching frequency provides a means to reduce the size and cost of these devices.

**Reduction in cooling requirements**
The significant reduction in heat sink temperatures by up to 50% has been observed with this technology allowing a reduction in heat sink size and/or the elimination of fans.

**Reduction in energy costs over the life of the equipment**
The usual temptation is to consider only the component and manufacturing cost of a system in calculating the value proposition. It is very important to consider energy savings when considering the value proposition of this technology. The energy cost savings over the life of the equipment is a significant, if not the dominant part, of the value proposition of this technology. This especially applies to solar inverter applications, where cost savings are dependent on inverter efficiency. A 40% to 50% reduction in power losses is a strong economic advantage.

*Author: Bob Callanan, Applications Manager*
*SiC Power Products*
*Cree Inc.*
www.cree.com





# WHITE GOODS TECHNOLOGY

## Creating More Energy-Efficient Home Appliances

By Dr. Stephan Chmielus

The rising cost of electricity will increase the consumer demand for home appliances that offer energy savings. However, this is only one consideration that consumers must consider when purchasing a new home appliance such as a washing machine or dishwasher.

The rising cost of electricity will increase the consumer demand for home appliances that offer energy savings. However, this is only one consideration that consumers must consider when purchasing a new home appliance such as a washing machine or dishwasher.

The lifetime and reliability are important aspects - in many cases, of equal importance as the consumption of electricity or water. It is obvious that the lifetime and reliability is oftentimes synonymous with the brand name of the home appliance. During the last decade a growing demand for home appliances with less impact on the environment in terms of electrical waste can be observed.

EcoDesign looks at all energy-consumption at each step. Furthermore it considers the whole life cycle costs including production and disposal costs. The directive established a framework for setting EcoDesign requirements and will force all manufacturers, which are building product applied from AC line to be energy efficient. To meet the EcoDesign requirements the mandatory technologies are summarized by different studies. The studies explicitly point out that only permanent magnet synchronous motors (PMSM) or high-efficiency induction motors fed with variable- speed drives are able to meet these energy-saving challenges. The potential savings of such drives are huge in case of variable-load applications and frequent start and stop cycles – commonly used in home appliances. However, not all motor applications can benefit from variable-speed drives particularly whe n only a constant speed is needed.

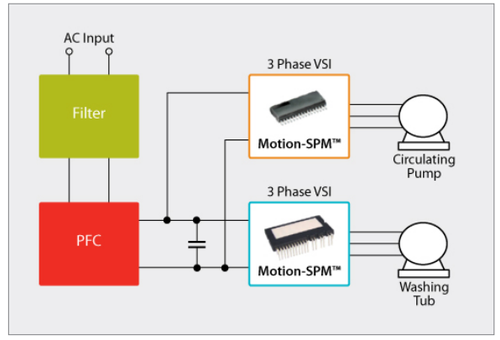



*Figure 1: Simplified Block Diagram of Washing Machine*

New technologies are the key to success in order to satisfy the requirements of energy-efficient home appliances. PMSMs are successfully replacing traditional motors. Figure 1 shows a simplified block diagram of a washing machine.

A washing machine for household is fed by single AC line followed by

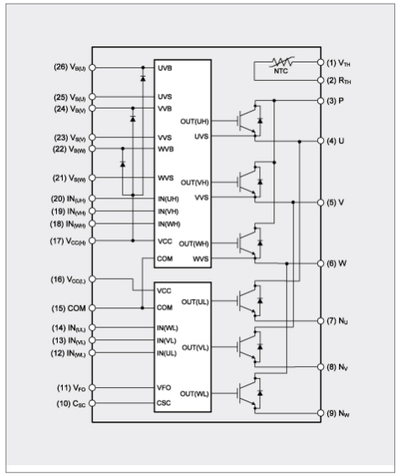



*Figure 2: Schematic of m-MiniDIP SPM module*

the required power factor correction either active or as in many cases passive. The new motor technologies require variable -speed drives. To enable such drives, designers have conventionally relied on discrete IGBT/ MOSFET solutions, which are now more and more replaced by intelligent power modules (IPM). IPMs are increasingly used since there are some significant benefits using integrated solutions. The recently launched m-MiniDIP SPM® (smart power module) is used as an example in the block diagram to drive the washing tub. It excels in the high integration of 3 half-bridges (Figure 2) including bootstrap diodes, NTC, fine-tuned gate drivers and additional protection functions as UVLP, SCP and fault output. To reduce the energy consumption of the module the stand-by current of the gate driver is decreased which enables to realize energy saving drives.

The precisely matched IGBTs and drivers ensure higher performance. Performance variations are much more controllable compared to a discrete solution. In addition the fully isolated module (39mm x 23mm) reveals increased reliability since the protection functions are close to the power switches and the low thermal resistance of the package results in lower temperature changes over a load cycle. The "failure in time" rate of this new family is comparable to the rate of one discrete IGBT. Hence the reliability of the module will outperform the discrete solution. Furthermore the wide range of junction temperature from -40°C to +150°C makes the module suitable for home appliances and for industrial applications.

To drive smaller motors like circulating pumps IPMs using MOSFETs instead of IGBTs are recommended. Especially for low output currents MOSFETs offer smaller losses compared to IGBTs due to the absence of the knee voltage and current tail. In addition the short circuit withstand time of MOSFETs can be up to one order of magnitude higher than the corresponding value of IGBTs. Therefore the use of MOSFETs is basically the preferred solution for low power appliances. TinyDIP SPM modules are a typical example of such IPMs. This integrated MOSFET solution is ideal for low power applications like pumps and fans since this fully isolated module can be placed very close to the motor. Even though the module size is only 29mm x 12mm, the maximum possible output power with a heat sink goes up to 200W, which cannot be reached with a IGBT- based solution of the same size. To simplify the "pick and place" assembly of this IPM it is also available as SMD packaging. In many cases, the use of such SMD IPM without heat sink is preferred. Now the maximum output power would be limit to roughly 90W but on the other hand manufacturing of the PCB is simplified. Both examples demonstrate that the use of IPMs can simplify the design of energy-saving drives due to an easier and faster design and higher flexibility.

The upcoming EcoDesign regulation of the European Union and its impact to energy-using appliances intensify the trend towards energy-efficient drives. Permanent magnet synchronous motors controlled with intelligent power modules have an important role to achieve the needed reduction of wasted energy. The example of a washing machine shows typical applications areas where the use of intelligent power modules can simplify and accelerate the design-in phase. These new solutions enable designers to develop cost-effective solutions for improving the overall environmental performance.

*By Dr. Stephan Chmielus*
*Fairchild Semiconductor Germany*

www.fairchildsemi.com





# AUTOMATED CONTROL

## Circuit Board DC-DC Power Supplies

By Randy Skinner

Modern appliances and equipment which utilize microprocessors, FPGAs and other complex ICs require accurate power supply voltages, often more accurate, in fact, than the tolerances provided by commodity low-dropout regulators (LDOs) and DC-to-DC power supplies.

Naturally, more precise power supplies are available, but at a premium price. The cost effective alternative is to use a separate power supply management IC to adjust the precision of one or more supplies at the same time. Providing a control signal to dynamically and continuously adjust a power supply's output voltage is referred to as closed-loop trimming.

Once the power supply is adjustable, other benefits can be realized. For example, a circuit board can also be tested for reliable operation over a range of voltage supply values. This is referred to as supply voltage margining. The adjustable voltage supply values can be used to simulate the expected precision of the power supply voltage, drift that can occur due to component aging, ambient temperature changes or fluctuations in supply load current.

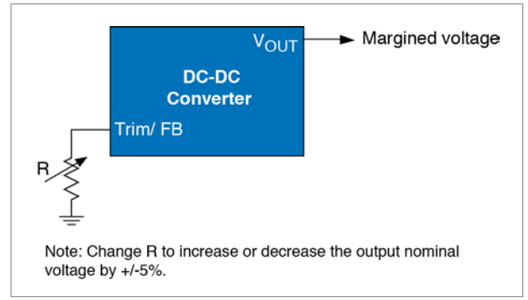



*Figure 1 - Supplies are margined by changing the resistor connected to the Trim/FB node*

**Voltage margining**

A voltage margining test ensures that the board is functional across the operating range of its on-board and input supplies. Circuit boards are also subject to other margining tests, such as temperature, timing and noise.

For example, if the allowed tolerance of a supply input is ±10%, the voltage margining test ensures that the board is functional when the input supply is at its margin-high (nominal voltage +10%) value and when its supply is at margin-low (nominal voltage -10%) value. If the board has a number of board-mounted supplies, then the margining test should also include the variation of individual board-mounted supplies. Margining tests typically are conducted during board debug. In some cases, Quality and Reliability departments will require margining before they will approve manufactured boards.

**Voltage margining implementation**

Figure 1 shows a DC-DC converter with a resistor connected to its

internal Trim/Feedback Node. The value of this resistor typically determines the nominal output voltage value of the DC-DC converter and is specified in the power supply's datasheet.

DC-DC converters usually require standard resistor values to set their output voltage to a standard value – e.g. 3.3V, 2.5V, 1.5V. To change the output voltage by +/-5% of their nominal operating voltage, designers use either a potentiometer for each of the DC-DC converters or a series parallel combination of standard resistor values. One has to manually implement the resistor change to all the boards that will be subject to testing in an environmental chamber. Due to delays and added cost, margin testing usually is not performed in a production environment. If it could be automated, however, it would become a powerful tool in verifying the reliable operation of a circuit board.

**Applications That Require Power Supply Trimming**

Trimming is required for circuit boards using ICs that require low supply voltages (1.2V or lower) with high current ratings (5A or more).

For example, a 1.2V DC-DC converter should guarantee a maximum of +/-5% (+/-60mV) variation under all of the following conditions:

• No-load to full-load average current variation

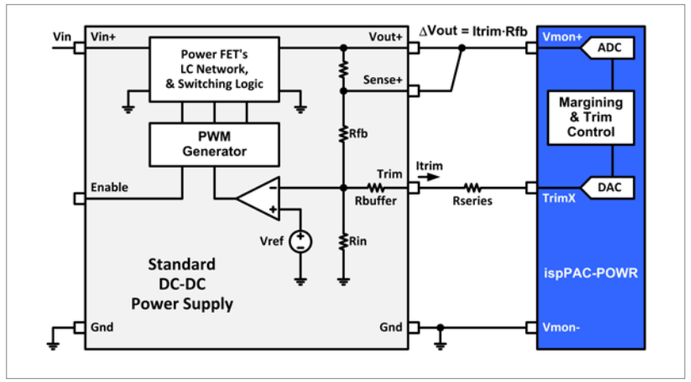



*Figure 2 - Supplies are margined by changing the resistor connected to the Trim/FB node*

• Output voltage ripple

• Dynamic power demands by the IC during different average current levels

• Component tolerances during manufacturing

In general, to meet the voltage device spec under all of the above conditions safely, the DC-DC converter requires an initial operating voltage accuracy of 2% or better. These high accuracy, low voltage supplies are usually more expensive and require high precision resistors to set the voltage.

Alternatively, the accuracy of a conventional lower cost DC-DC converter can be improved by using an external trimming mechanism. The next section describes trimming using a Lattice Semiconductor power management IC. Similar products are also available from Maxim, TI and Analog Devices. The Lattice Semiconductor products will be used here to explain the basic principles of trimming and margining.

**Trimming and Margining – Principle of operation**

Figure 2 shows a Lattice Power Manager II device implementing trimming and margining functions for an analog DC-DC converter.

On the top portion of Figure 2 is a DC-DC converter supplying power to its load. The output voltage is determined by the components used in its feedback circuitry. The Power Manager II device on the right measures the DC-DC output voltage using the on-chip ADC though differential sense inputs (Vmon+ and Vmon-). The Power Manager II can increase or decrease the output voltage of the DC-DC converter by increasing or decreasing its trim voltage with its on-chip DAC, thus changing the current applied to the DC-DC converter's feedback node.

A setpoint register in the Power

Manager II control circuitry holds the required voltage value at the load. Once every 580us the Power Manager II device measures the voltage at the load using its on-chip ADC. The digital output of the ADC is compared against the setpoint register contents. If the load voltage is higher, the DAC contents are decremented, which in turn reduces the voltage applied to the feedback node of the DC-DC converter. If the load voltage is lower, the DAC contents are incremented, applying higher voltage to the node. This is called the closed loop trim mechanism.

It is possible to break the closed loop trim and load the DAC register directly through the I2C bus to the Power Manager II device. This method is used to implement margining. An external microprocessor directly loads a pre-selected DAC value into the Power Manager II, which will result in changing the output voltage by, for example, +/-5%. The microprocessor can also measure the output voltage of the DC-DC converter using the Power Manager II's ADC, and tweak the output voltage up and down as needed to implement closed loop margining. In a circuit board, there typically are multiple types of supplies providing different supply voltages. These individual supplies require different current levels to be injected into their feedback nodes. This in turn requires a unique resistor network for each type of DC-DC converter

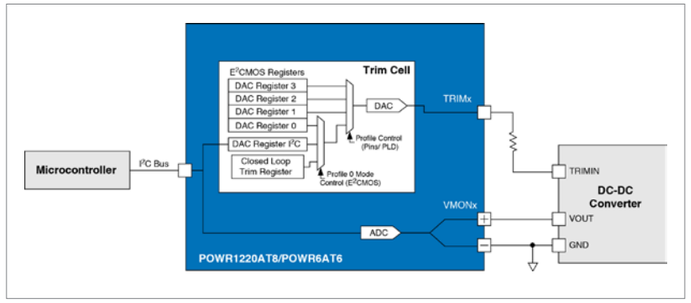



*Figure 3: Closed loop trimming and margining using a microcontroller*

to be connected between the Power Manager II and the DC-DC converter feedback node.

**Closed loop trim and closed loop margining using a microcontroller**

Figure 3 shows the configuration used for closed loop trimming with a microcontroller. Here the microcontroller measures the DC-DC converter output voltage periodically, using the on-chip ADC through the I2C bus. The microcontroller then algorithmically calculates the new DAC value depending on the DCDC converter voltage and loads the new DAC code through the I2C interface.

The microcontroller-based margining is implemented entirely through the I2C bus and uses profile 0 in the Power Manager II. To implement closed loop margining, the microcontroller loads the starting DAC code into the DAC register via I2C and waits for the ADC voltage to stabilize. Depending on the stabilized voltage value, the microcontroller increments or decrements the DAC code. This method enables setting and controlling the margined voltage accurately.

**Designing trimming and margining networks using PAC-Designer software**

Determining the required resistor topology involves finding a solution for a number of nodal equations and an understanding of the error amplifier architecture of the DC-DC converter. In addition, the design can be iterated until the solution yields standard resistor values.

The Lattice PAC-Designer software automates the process of determining the resistor topology while using standard resistors in the resistor network. More details on interfacing Power Manager devices to various types of power supplies and how PAC-Designer design software simplifies that task are available online at www.latticesemi.com. An excellent reference showing more detail can be found in Lattice application note AN6074, Interfacing the Trim Output of Power Manager II Devices to DC-DC Converters.

**Summary**

The use of widely available power management control ICs, such as those available from Lattice Semiconductor (Power Manager II and Platform Manager product families) enable the use of commodity priced DC-DC and LDO power supplies to deliver precision voltage performance. In addition, testing techniques such as power supply margining are made available via I2C control once the supplies are in a control environment.

Devices from multiple vendors are available ranging from simple 1 to six supplies. Lattice provides two families of power and board management devices with up to eight trim power supply trim outputs. Also integrated in the same Lattice devices are other power and board management functions, such as supply sequencing and monitoring, supervisory functions, reset generation, hot swap and more.

*By Randy Skinner, Staff Product Marketing Engineer*
*In-system programmable mixed*
*signal products*
*Lattice Semiconductor Corp.,*
*Hillsboro, Oregon*

www.latticesemi.com

# INTEGRATION IN EMBEDDED HMI

## Combining graphic display controllers with touch-screen and USB peripherals

By Rishi Vasuki

The new MCUs promise to combine lower system cost, with a wider range of options for higher system integration. However, while they enable designers to lower the cost of system hardware, manufacturing and inventory, the increased complexity of software development can impact on time to market and demands a robust integration of touch-sensing and other human-interface functions onto a single MCU.

HMI designs in embedded systems are evolving fast as the cost of manufacturing fashionable and more elegant interfaces continues to decrease. Some appliances are already combining touch-sensitive interfaces, such as keys, sliders, touch-screens and haptic feedback, with rich graphical displays using the latest generation of microcontrollers (MCUs) which integrate graphic display controllers, with peripherals for implementing capacitive-touch, touch-screen controllers and USB onto a single chip.

First, consider the origin of these concerns. Take, for example, capacitive touch-sensing. When touch-sensitive keys were first introduced, designers soon realised that they were not as simple to implement as traditional push-buttons. Touch-sensitive keys have to be handled in the same way as analogue sensors: Radiated noise, or noise that may be conducted from environmental sources such as common appliances, compact fluorescent lamps, power supplies, cell phones and motors, needs careful management. To achieve robust and responsive keys, software techniques such as envelope detection, filtering,

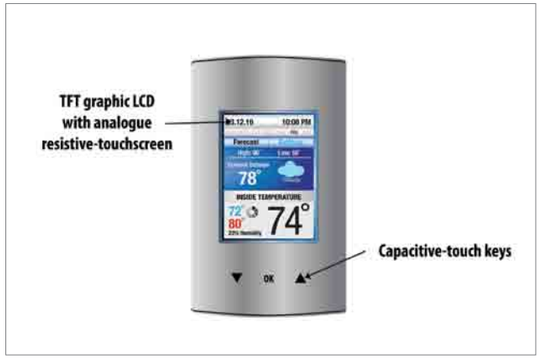



*Figure 1: Thermostat with resistive- and capacitive-touch technologies*

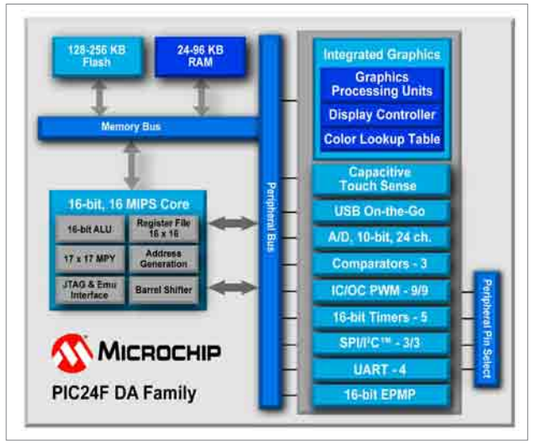



*Figure 2: High-integration MCU with graphics controller, touch-sensing and USB*

de-bounce and slew rate filters have to be applied, in addition to ensuring a good layout for signal acquisition. Now, the need to refresh a segmented or graphical LCD, when a user input is received, must be added to this human-interface system. Rendering graphical constructs, such as geometrical shapes or text, onto a display, such as a TFT or OLED, has historically needed processor bandwidth. Also, consider human-interface applications that incorporate touch-screen input in addition to the graphics display and the touch-sensitive keys, such as the thermostat in Figure 1. Finally, a communication interface, such as USB, will typically be required.

The challenge, therefore, is to enable real-time processing of the user inputs derived from touch-sensitive keys, a touch-screen sensor and USB data communication as well as updating the display. The solution falls into two categories which are central to the underlying hardware and software.

**Hardware implementation**

There are a number of MCUs that combine an LCD controller and touch-sense peripheral on a single chip but, typically, the LCD controller drives a segmented display rather than a graphics LCD.

The latest generation of MCUs, such as the PIC24FJ256DA210, shown in Figure 2, takes integration to a new level by combining a graphical display controller, a USB 2.0 On-The-Go peripheral and a special analogue peripheral that can be used for touch-sensing. To support graphics displays, the PIC24FJ256DA210 has a built-in colour look-up table, a large 96KB RAM, a graphics processing unit (GPU) and a direct interface to STN, TFT and OLED displays. The large on-board RAM allows 256-colour graphics data to be stored, at 8-bits per pixel, for a 320x240 QVGA display within the on-chip RAM. Colour palettes, used in the colour look-up table, can also be switched to use a different set of 256 colours across different image frames. The GPU allows simple objects, such as lines, rectangles, ASCII text and PNG-like image decompression, to be rendered by issuing a single command. This reduces the CPU overhead to zero.

Figure 2 also shows the Charge Time Measurement Unit (CTMU) analogue peripheral. Capacitive touch-sensing is one of many applications supported by the CTMU peripheral. The CTMU provides a constant current source with a timer that can be used to charge a sensor pad. The voltage on the pad can be measured by the on-chip Analogue-to-Digital Converter (ADC). When a user's finger is placed on the pad, the capacitance change at the sensor pad is recorded as a change in voltage by the ADC. In the simplest implementation, each ADC channel can be connected to a touch-sensitive key input. With 24 ADC channels, the PIC24FJ256DA210 provides sufficient capacitive-touch channels to cover the needs of most applications.

There is one further hardware consideration: If the application has both a resistive touch-screen input as well as touch-sensitive keys, for short-cut menu functions, the graphical LCD is overlaid with a resistive touch-screen sensor. If the touch-screen controller is integrated

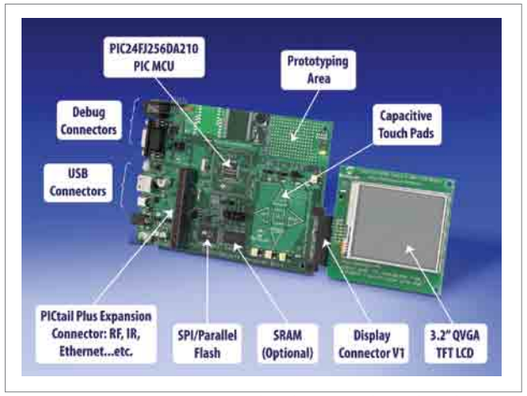



*Figure 3: PIC24FJ256DA210 development board with 3.2" TFT display kit*

onto the main MCU, the touch-screen sensor outputs, which are typically 4 or 5 wires, may be connected to the MCU's analogue channels. In this case, the ADC resource on the MCU is shared between the touch-sensitive key functions and the touch-screen function. The ADC measurements are used to estimate the X & Y coordinates sensed on the touch screen.

**Software implementation**

Typically, the firmware for the graphics display drivers and capacitive touch-sensing will be available as separate libraries. For an effective integration of these libraries, a main routine is required, functioning like a basic Real-Time Operating System (RTOS), to establish the priority and frequency of servicing each task. For tasks which share common hardware resources, the main routine also needs to establish a mechanism for non-destructive updating of the control and data registers for the shared resource, prior to switching between tasks. In the example above, both the touch-screen sensors and the touch-sensitive keys feed into the ADC. The rate of sampling the ADC, the channels being sampled and the number of samples needed, differ across the touch-screen sensor and the keys. Therefore it is necessary for the main routine to save these parameters before switching between the two tasks.

Since the user may, at any time, provide input to either the touch-screen or the keys, the main routine may need to use time-slicing to enable both sensors to be scanned frequently enough. The display may need periodic updates if, for example, the application is rendering animated graphics on the screen. If the display is only updated when the user makes menu selections, then there is no CPU resource contention between the touch-sensing and display-driver functions. As the example device (PIC24FJ256DA210) has dedicated graphics acceleration hardware, time-slicing between the touch and graphics functions is less of an issue. On this device, rendering a box, a line or ASCII text simply requires a single command to be issued by the CPU. A demonstration project that showcases the integration of the touch-sensitive keys, the touch-screen sensor and the graphics display, using underlying software libraries, is available for free download with the mTouch™ Capacitive-Touch library and can be run on the PIC24FJ256DA210 development board shown in the Figure 3.

There are other functions that may be integrated on a single chip, together with touch-sensing. For example, the CTMU peripheral can be used for temperature-sensing, medical instrumentation, time measurement or other functions. In an application such as a thermostat, it is possible to use the CTMU peripheral for temperature sensing, in addition to touch-sensing, by using an external diode. Since temperature measurement only needs to be carried out infrequently it is possible to share this peripheral across these two functions.

**USB communications**

Integrating USB with touch-sensing is relatively easy if simple rules are followed. When the application is connected to a USB host, it goes through an enumeration phase during which the CPU bandwidth may be largely dedicated to performing the USB function. Touch-sensing functions may be re-started in a couple of minutes, once the enumeration phase has been completed. Once enumeration is complete, the USB functions consume a very small amount of the CPU bandwidth, typically under 2%. At this point, the main routine may choose to service the USB receiver function periodically, every millisecond or so, or switch to a more interrupt-driven approach.

Many applications with touch-sensitive interfaces have begun to incorporate haptic feedback. Integrating haptics into an application is more of a mechanical challenge. Typically, haptics require a simple Pulse Width Modulation (PWM) peripheral to drive a small vibrator or motor. It is conceivable that, in some applications, the on-chip PWM peripheral is also being used to drive an audio speaker. In such cases, an effective integration may require having separate time-bases for the PWM channel that is driving the haptics motor and the one driving the audio speaker.

**Conclusion**

Whilst single-chip integration of graphic display and touch-sensing features can lower system cost, software complexity can be a real factor in the time to market. Implementation is simplified by selecting an MCU platform which is supported by graphics, USB and touch-sensing software libraries that have been designed and tested to be inter-operable and where robust integration has been demonstrated.

*Author: Rishi Vasuki, Product Marketing Manager*
*Advanced Microcontroller Architecture Division*
*Microchip Technology*

www.microchip.com

# RELIABILITY IN WHITE GOODS

## Designing systems for today's home appliances

By Graeme Clark

The demands being placed on designers for the next generation of domestic appliances are increasing drastically. Today we see many conflicting demands to use less power, less water and to create less noise, naturally all for less cost.

These requirements create the need for more complex electronics to control the appliance and, of course, more complex software to control the electronics. This makes it essential that all of us in the industry ensure these complex systems are both safe and reliable to use.

In this next generation of smarter, greener domestic appliances, we are being driven by the new sophistication of the electronics themselves to develop safer and more reliable systems. However, another reason for this trend is new legislation from the European Union, such as the IEC60730 standard for safe and reliable product design, to make sure this happens.

To support this requirement, Renesas Electronics has introduced a new set of advanced safety peripherals and functions on its next generation of microcontrollers aimed at white goods applications. Several of these features have been included in the new RX200 family, a new generation of 32-bit microcontrollers for white goods and motor control applications. These devices combine the processor performance required for the next generation of smart appliances with large, embedded on-chip memories and the peripherals required for white goods applications. Most importantly, these devices integrate many innovative features to allow developers to easily implement applications which are both reliable and support built-in self-tests.


*Figure 2: High-integration MCU with graphics controller, touch-sensing and USB*

The first device in this new family, the RX210, is shown in figure 1. The RX210 is a sophisticated device that supports many advanced peripherals and integrates a large on-chip flash memory and SRAM.

The RX210 implements a range of basic system reliability functions. These include a Power-on-Reset circuit to make sure the device powers up correctly in every circumstance, and a programmable low voltage detection system. This

allows the designer the flexibility to detect and deal with a range of brown-out conditions, using internal voltage references to monitor both the device's Vcc levels and potentially the level of the external power supply.

To minimise the risk of errors in the user's software, the RX210 implements two on-chip watchdog timers. One uses the standard CPU clock, while the second can select an independent internal clock source, allowing it to operate even when the system clocks fail. It also has a window function to allow the detection of system failures that cause the watchdog to be continuously reset, and of conditions that would make the watchdog timer time out.

The RX210 also has an on-chip temperature sensor which can detect abnormal temperatures during operation, perhaps indicating an overheating problem in the system.

Other standard functions allow the user to detect whether the device's I/O pins are not being driven correctly and to check that the voltage level being driven out is actually present on the I/O pins themselves.

Similar system test functions have been integrated in the analogue to digital converter (ADC). The ADC has been designed with precharge and discharge circuitry that operates before the ADC conversion is made to check if the pin is open or short circuited. Internally, the ADC has been designed with self-test functions, giving users a number of internal references inside the ADC to test that it is operating correctly. Users can also put the ADC into a test mode to check an external signal. Here, the ADC will also save the value produced by the conversion of an additional internal reference signal, enabling the user to minimise the risk of a problem with the ADC at a later date.

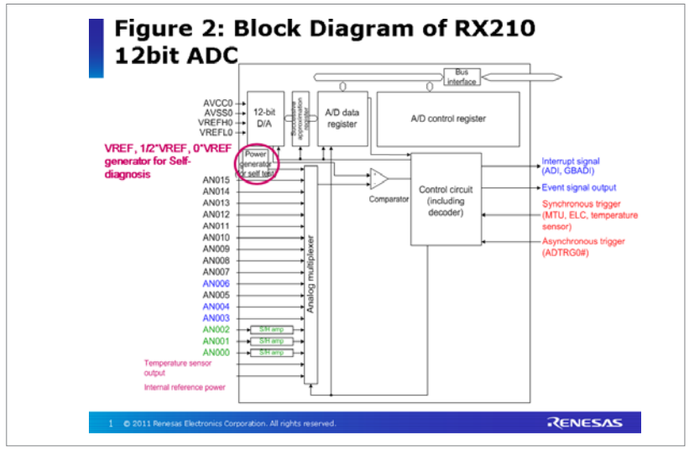



*Figure 2: Block Diagram of RX210 12bit ADC*

Turning to some of the other systems on the RX210, an important peripheral inside the device is the Data Transfer Controller (DTC). The combination of the DTC and some of the device's intelligent peripherals allows the user to automate many of the more complex self-test functions, especially those required to test the on-chip memory. These tasks traditionally take up significant amounts of CPU bandwidth. The new architecture used on the RX210 allows the CPU to concentrate on more important tasks, only responding if an error is detected. For this reason, the DTC underpins many of the "smart" functions implemented on the RX210.

**Data Transfer Controller (DTC)**

The DTC is a powerful method of transferring data from a location in memory to a peripheral on the device. Like an interrupt, it can be triggered by any event on the device. So any peripheral event, such as a timer overflowing, an external interrupt pin changing, or the ADC conversion finishing, can cause an automatic data transfer to be initiated. This transfer can move one or more bytes from any location in memory or a peripheral to any other location. It is also not limited to the peripheral that generated the transfer request. A frequent use for this function is to make a transfer between memory and a peripheral, such as the Digital to Analogue Converter (DAC) under the control of another peripheral, such as a timer.

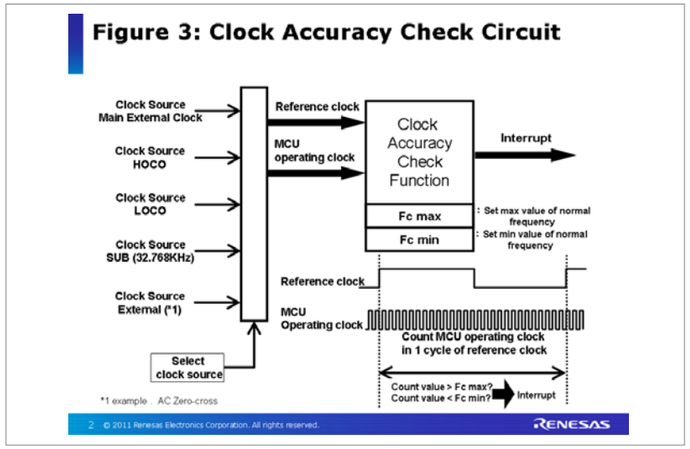



*Figure 3: RX210 Clock Accuracy Check Circuit*

The Data Transfer Controller can be used in many ways, generating multiple transfers of one or more bytes, or single transfers that occur once. One of the most important features of the Data Transfer Controller is its ability to chain transfers. This enables one transfer to automatically trigger a second, which, when complete, can trigger a third, and so on. This allows the user to create a sequence of events moving data around the device, without CPU intervention. This is a very powerful feature when combined with some of the following peripherals.

**CRC Function**

A hardware CRC function is implemented on the RX210 and can be used in a variety of ways with three user selectable polynomials. However, when combined with the Data Transfer Controller and a timer, it provides a powerful mechanism to allow the system to automatically cycle through the memory in the background, while the CPU is running normally, and check that the flash is still programmed with the expected data.

**DOC Function**

The Data Operations Circuit (DOC) is a power circuit that allows the user to make simple comparisons between two elements of data without CPU intervention. This is probably one of the most flexible and powerful safety features on the device, as it assists RAM failure testing and can also be extremely useful in other applications.

The DOC can execute three simple operations. It can make a comparison between two elements of data, then generate an interrupt depending on whether there is a match or not. It can also add or subtract values and generate an interrupt if the result is an overflow or underflow respectively. These addition or subtraction modes enable the detection of a range of values, a useful feature in many applications.

When combined with the Data Transfer Controller, the DOC is able to operate in the background, automating many tasks independently of the CPU. One possible task is to test some areas of the SRAM with minimal CPU intervention, but many other applications are also possible.

These are just some of the advanced features implemented on the RX210 to support the next generation of white goods applications. They facilitate the development of extremely reliable, cost-effective solutions for home appliances and easily meet both today's and tomorrow's regulatory requirements.

*Author: Graeme Clark*
*Product marketing Specialist, Industrial Business Group*
*Renesas Electronics Europe*
www.renesas.com

# CIRCUIT PROTECTION CONSIDERATIONS

## Electronic Components in Household and Professional Appliances

By Barry Brents and Matt Williams

The power supplies, relays and other electronic components found in household and professional-grade appliances can benefit from the application of resettable overcurrent protection.

Polymeric positive temperature coefficient (PPTC) devices offer low resistance and are compatibly sized with fuse solutions. Like traditional fuses, they limit the flow of dangerously high current during fault conditions. The PPTC device, however, resets itself after the fault is removed and power to the circuit is cycled, obviating the need to replace a blown fuse.

Protecting increasingly sophisticated and complex control boards from misconnection, power surges or short circuit damage is also of particular concern to the equipment manufacturer. Although appliance transformers, their enclosures and connections are capable of withstanding higher voltage transients, the use of sensitive solid-state devices on the board necessitates improved overcurrent and overtemperature control.

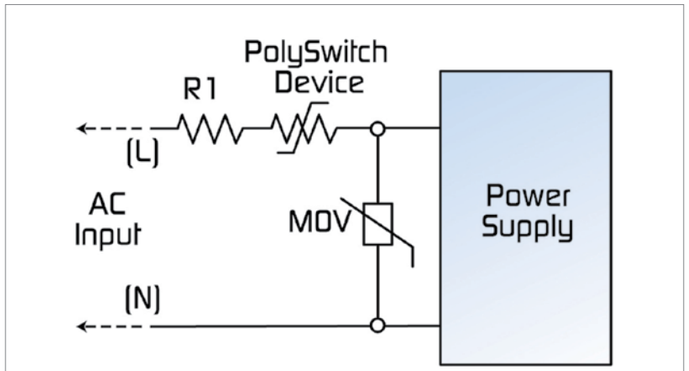



*Figure 1: Typical circuit protection design for switch-mode power supplies.*

A coordinated circuit protection strategy can help protect equipment from damage caused by excessive currents during a fault or overload condition, as well as voltage spikes or exposure to steady-state overvoltage conditions.

**SMPS Design Considerations**

Switch-mode power supplies (SMPS) offer the size, weight, and energy-saving advantages required for consumer electronics and have continued to replace linear-regulators in many applications, including white goods. However, because SMPS lack the inherent resistance of prior generation designs, they often require more robust circuit protection.

PPTC overcurrent protection devices can help manufacturers meet UL60950-1/LPS (Limited Power Source) requirements for SMPS and improve equipment safety and reliability. While these devices cannot prevent a fault from occurring, they respond quickly, limiting current to a safe level to help prevent collateral damage to downstream components. Additionally, the small form factor of PPTC devices makes them easy to use in space-constrained applications.

The PPTC device has a low-resistance value under normal operating currents. In the event of an overcurrent condition the device "trips" into a high-resistance state. This increased resistance helps protect the equipment in the circuit by reducing the amount of current that can flow under the fault condition to a low, steady-state level. The device remains in its latched position until the fault is cleared. Once power to the circuit is cycled, the PPTC device resets and allows current flow to resume, restoring the circuit to normal operation.

As shown in Figure 1, a PolySwitch™ PPTC device can be installed in series with the power input to help protect against damage resulting from electrical shorts, overloaded circuits or customer misuse. Additionally, a Metal Oxide Varistor (MOV) placed across the input helps provide overvoltage protection.

The PolySwitch device may also be placed after the MOV. Many equipment manufacturers prefer protection circuits combining resettable PPTC devices with upstream fail-safe protection. In this example, R1 is a ballast resistor used in combination with the protection circuit.

**Solenoid Design Considerations**

A solenoid is an electromagnetic device consisting of a coil assembly, frame, armature, and backstop. The coil assembly and backstop are mechanically secured within the frame and the armature is inserted into the assembly. When the coil is excited with current, a magnetomotive force is created, causing the plunger to be pulled into the coil and seat on the backstop.

Once the solenoid is energized, the end of travel is detected by a sensor. The sensor then feeds back the position of the armature to the system electronics, turning off the power to the solenoid. Should the sensor fail, causing the armature not to pull in, the intermittent solenoid will generate excessive heat and may fail.

Installing a PPTC device in combination with an MOV on the primary side of the AC input can help protect against damage caused by overcurrent and overvoltage faults. Unlike a single-use fuse, the resettable PPTC device also helps protect against damage resulting from conditions where faults may cause a rise in temperature with only a slight increase in current draw.

Certain overload conditions may cause the MOV to remain in a clamped state where it will continue to conduct current. This may eventually result in an overtemperature failure of the device. Placing the PPTC device in series with and in close thermal proximity to the MOV can help protect that MOV in extended overload conditions – by transferring heat to the PPTC device. This causes the PPTC device to trip faster, limiting the current through the MOV.

This technique lets designers leverage the temperature response of the PPTC device and replace other thermal protection elements in the circuit. Not only does the PPTC device perform dual functions in this case, it also provides a fully resettable solution. Probably the most common cause of solenoid failure is mechanical blockage. This can occur when the solenoid becomes contaminated with dirt or debris that lodges between the armature and the inside of the coil, blocking proper movement. Other problems include misalignment, broken springs or an opposing force.

Any of these conditions can cause constant current to be ap

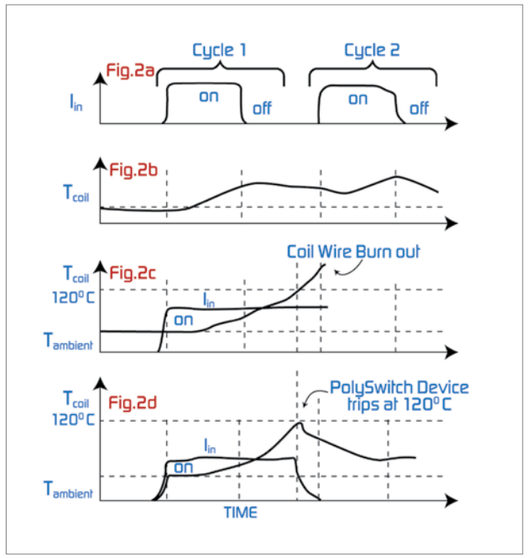



*Figure 2: PolySwitch device helps prevent overcurrent/ overtemperature damage by limiting current to coil.*

plied to the solenoid, increasing coil temperature and ultimately burning the coil insulation and wires. As shown in Figures 2a and 2b, during normal conditions, the coil temperature increases each time the solenoid is cycled. Figure 2c illustrates how an overtemperature fault may cause the coil windings to burn out. Figure 2d shows how a PolySwitch device inserted in the circuit will trip at approximately 120°C, limiting IIN so that the coil temperature gradually drops and helps prevent damage to the coil.

**Relay Design Considerations**

Relays are frequently used in consumer electronics to control high currents and voltages with lower signal levels, or to switch currents that must be isolated from the control circuit. A relay's most basic components are its coil, armature, and contacts. When the relay is put into a circuit, the current from that circuit induces a magnetic field in the relay coil. The magnetic field then affects the armature in such a fashion that it causes the contacts to make or break the part of the circuit that is attached to the relay output.

Relay damage can result from excessive voltage or current. A common problem can occur when a relay interrupts current to an inductive load and causes a voltage spike. If the voltage spike is severe enough, to exceed the relay's contact voltage rating, the contacts can be damaged (V = Ldi/dt). This damage may occur suddenly or slowly, over many years of operation.

Additionally, excessive current through the relay contacts can cause damage when the contacts open and the current is interrupted. Excessive currents and voltages can also damage the relay coil. If a relay coil is designed to be energized for only a short duration in normal operation, normal operating current may eventually harm the coil if it is accidentally energized for an extended period of time.

Figure 3 shows a typical relay protection circuit. A PolySwitch device is placed in series with the relay coil to limit the current to the relay in case of a fault or accidental overload. This figure also shows a PolySwitch device in series with the relay contacts.

It is important to choose a PPTC device with a voltage rating equal to or greater than the maximum expected voltage. The device must also have a hold current equal to or greater than the maximum steady-state current in normal operation. Additionally, the maximum ambient temperature must be taken into account because the hold current decreases as the ambient temperature increases. Figure 3 also shows an MOV or MLV in parallel with the relay contacts. These devices are rated according to voltage and maximum surge current. It is important to select a device that will not conduct significant current at the normal peak voltage. MOV specifications include a maximum allowable AC or DC voltage. Each MOV and MLV device also has a maximum surge-current rating. The usual standard for rating surge currents uses an 8/20 microsecond wave shape (i.e., an 8-microsecond rise time, and a 20-microsecond delay time to half the peak value). As the varistor size increases, the 8/20 microsecond surge current rating increases. An MOV or MLV can also be used in parallel with the relay coil, as shown in Figure 3.

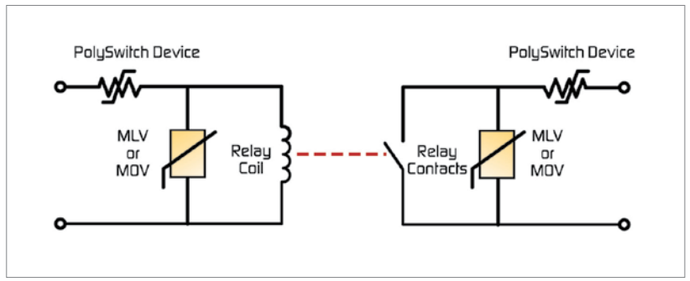



*Figure 3: Typical overcurrent/overvoltage relay protection circuit.*

**Summary**

Coordinated overvoltage/overcurrent circuit protection can help designers reduce component count, provide a safe and reliable product, comply with regulatory agency requirements and reduce warranty and repair costs. PPTC devices offer resettable functionality and low resistance in the circuit. They are rated to 240 VAC, permitting maximum voltages of up to 265 VAC and can be installed in the AC input lines. MOV and MLV devices help manufacturers meet a number of safety agency requirements, and provide high current-handling and energy absorption capability as well as fast response to overvoltage transients.

*By Barry Brents and Matt Williams*
*TE - Circuit Protection*

www.circuitprotection.com

# DIGITAL POWER CONTROL IMPACTS POWER DESIGN ON MANY LEVELS (PART 2)

By David G. Morrison

Demands for consumer-friendly features and energy-saving operation translate to increasing electronics content in each new generation of appliances and white goods. Naturally, the power systems within these applications are becoming more sophisticated, particularly in the area of motor control where digital control schemes are playing a central role in enabling quieter, more-efficient operation.

Engineers developing motor control solutions for these applications will need to have greater knowledge of digital control techniques as time goes on. The same may be said for power electronics engineers working outside the white goods industry, as digital power control continues to make its way into numerous other applications.

Last month, we discussed the impact of digital power supply controller ICs on power design, both as it affects requirements for design skills at the chip level as well as at the power supply and power system levels. In this column, we explore some of the effects of DSC/DSP-based power supply and power system design on engineers working in these areas. We'll also look at some of the general requirements for power designers working with digital power control, and how future technology developments may impact power design work involving both dedicated digital power controllers and DSPs/DSCs.

**DSC-Based Design Requires Greater Knowledge of Digital Control**

If even designers who use GUIs to configure their state-machine-style digital power controllers may require some understanding of the underlying digital design, then it's to be expected that power supply designers using the more-programmable DSPs and DSCs will need even greater familiarity with digital design techniques.

Power supply designers (or members within a given design team) who use DSCs and DSPs will typically have some understanding of control theory including digital control theory, says Bill Hutchings, a product marketing manager with the High-Performance Microcontroller Division of Microchip Technology. There's also the expectation that the design team will require some experience with software development. According to Hutchings, a power supply design team that is transitioning from analog power control to digital control using DSCs will typically add members who are more adept at developing software and "who understand about PWMs and the control loops they need."

However, power supply engineers implementing digital control on DSPs and DSCs are usually not starting from scratch. Hutchings notes that his company provides reference designs that include control loops and topology control software. "Typically, they end up modifying the reference design to their particular power needs," says Hutchings. This could mean selecting pieces of the reference design that correspond to the parts of their power supply in which they want to employ digital control.

And in most cases, the designers will be changing parameters of control loop operation. "Typically, the basic control loops stay the same, but the designers have to tune the parameters in the software to get the responses that are in their power supply specification. For example, there are parameters within the code for response time and how the power supply operates under different load conditions," says Hutchings.

Hutchings comments that designers do not need to be DSP experts to customize the code for their applications. However, "the more knowledgeable they are on how to tune digital PID loops, the faster their implementations will go."

**Don't Overlook Microcontrollers or Ignore Analog**

Both Hutchings and David Williams, the director of systems engineering at CHiL Semiconductor, note the importance of understanding microcontrollers, not only for those designing digital control loops, but for power supply designers working in all areas. Williams comments that designers "need to know how to program microcontrollers. We've seen those for ten years on power supplies over and over again. They pack a lot of functionality into a small size." That functionality involves housekeeping and other types of system controls, observes Hutchings.

While the focus here is on digital design, it almost goes without saying that most everything engineers have learned as analog power designers is still relevant. In terms of the control side of the design, the analog experience provides a basis for understanding what the new controllers will be trying to do digitally, whether you're using a state-machine type or DSP/DSC-style controller. And as Patrick Le Fevre, marketing and communication director of Ericsson Power Modules says, "you still need very good knowledge of analog power to design the power train. You can try to model everything, but in the end, you need to use MOSFETs, a transformer, and a lot of physical components that you cannot always model." Plus, there's the board design.

Dr. Ali Shirsavar, director of Biricha Digital Power, a company that provides digital power supply design workshops, places analog design skills at the top of his list when discussing the knowledge required to successfully implement digital power control using DSPs.

"To implement good 'stable' digital power supplies, designers need a good understanding of three main subjects," says Shirsavar, who identifies 1) analog power supply unit design, 2) discrete time control theory and 3) real-time embedded systems programming as the critical subjects.

"The problem is that although most power supply designers know number one well and will have studied both subjects two and three at university, they will rarely have needed to use discrete time control theory or programming for all the years that they have been working as "analog" PSU designers," explains Shirsavar.

One bright spot for analog power supply designers looking to gain proficiency in the design of digitally controlled power supplies is that the learning curve is not necessarily a long one.

"Discrete time control theory takes surprisingly little time because although at university students spend months studying this vast subject, for digital power supplies you only need a tiny tiny subset of it; the trick is to know which tiny part you need to learn," says

Shirsavar. In his company's digital power seminars, "We teach engineers everything they need to design a stable discrete time controller for their digital power supply in one afternoon."

With regard to the third subject, embedded systems programming, the commitment needed to master the topic is harder to predict. "If they just need a few power supplies, then the code is quite simple and during the workshop we teach them how to do it plus give them all the templates, fully running DSP code/libraries, etc. But if then they also want communications, condition monitoring, and GUI on top, then obviously the code will get more complex."

**Looking ahead**

For many power electronics engineers, there is still time to learn about digital power control because the transition to digital power in the industry at large is a gradual one. "Right now, the volume of applications for digital power outside the information and communications technology industry is relatively little compared to what it is in the telecom-datacom industry," says Le Fevre. "I believe it will probably take five to ten more years before the rest of the industry starts to use digital power, and there are a number of applications where analog works perfectly for its purpose. Digital power will not replace analog everywhere." Nevertheless, as usage of digital power control becomes more widespread over the next five to ten years and beyond, power designers will be expected to understand the technology at a deeper level. However, as Hutchings describes it, this requirement will evolve naturally.

"Digital control of power products will greatly expand in the coming years and will become the norm," says Hutchings. "As the use of the technology is expanded, and the knowledge base built up across many different market segments, the foundations of the control algorithms will shift such that the only way they can be done practically is digitally. So, the needs for digital-control knowledge and design skills, particularly in-depth knowledge and skills in this area, will only increase."

For examples of power electronics engineering positions with requirements for experience in digital power control and other digital design skills, see the online version of this article.

About the Author


David G. Morrison is the editor of How2Power.com, a site designed to speed your search for power supply design information. Morrison is also the editor of How2Power Today, a free monthly newsletter presenting design techniques for power conversion, new power components, and career opportunities in power electronics. Subscribe to the newsletter by visiting www.how2power.com/newsletters.

*Author: David G. Morrison*
*Editor*

www.How2Power.com

# DOMESTIC EFFICIENCY

By Cliff Keys, Editorial Director & Editor-in-Chief, Power Systems Design

It's difficult to consider white goods as green. But that's the way it's going. Not just through government regulations either. Manufacturers are seeing that there is a clear advantage in producing energy efficient consumer products, and with the price of energy rising, this is not surprising.

For our industry, it means that efficient products can turn this industry around, and it's happening already. Manufacturers are able to sell on value and not just on price. Apart from a higher efficiency classification, better components adopted in the design can mean better reliability, which can be a brand differentiator.

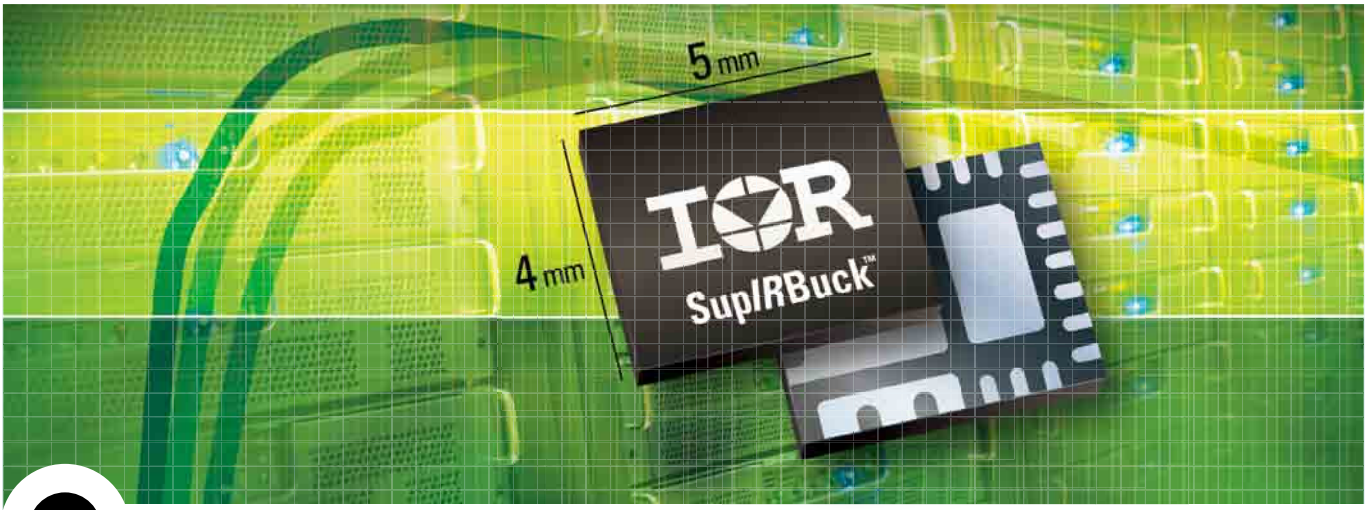
**Solar inverters**

Global PV inverter revenues reached $1.6 billion in Q4'10, 24% lower than the previous quarter, but 30% higher than in Q4'09, according to IMS Research's latest quarterly report on the market. Factory-gate prices also fell in the quarter by 4%, although shipments remained robust despite cooling demand and high inventory levels. The report, which is based on actual sales and shipment data from 35 of the largest PV inverter suppliers, including the largest Chinese vendors, revealed that 2010 did not see the typical end-of-year rally; and shipments of inverters fell substantially in Q4. A further slide in shipments and revenues is also estimated for Q1'11 because of very high customer inventories and low demand in Europe.

Germany's dominance in this market is starting to wane; share of inverter shipments has fallen steadily over the past five quarters as other international markets have taken off. Germany accounted for more than half of all inverter shipments in Q4'09, but this fell to just 35% in Q4'10. Despite this, EMEA's share of global PV inverter shipments remained stable in 2010, consuming more than 80% of total industry shipments in the year. Germany's falling share was also apparent in the results of its supplier base, with many German suppliers losing market share globally. The biggest market share loser last year according to IMS Research was market leader SMA Solar Technology which shed 5% despite doubling its sales.

So, with Europeans increasingly cladding their rooftops with solar panels and becoming sensitized to selecting energy efficient appliances, even at a premium; this must be good for the improvement of our environment, and for our industry's business.

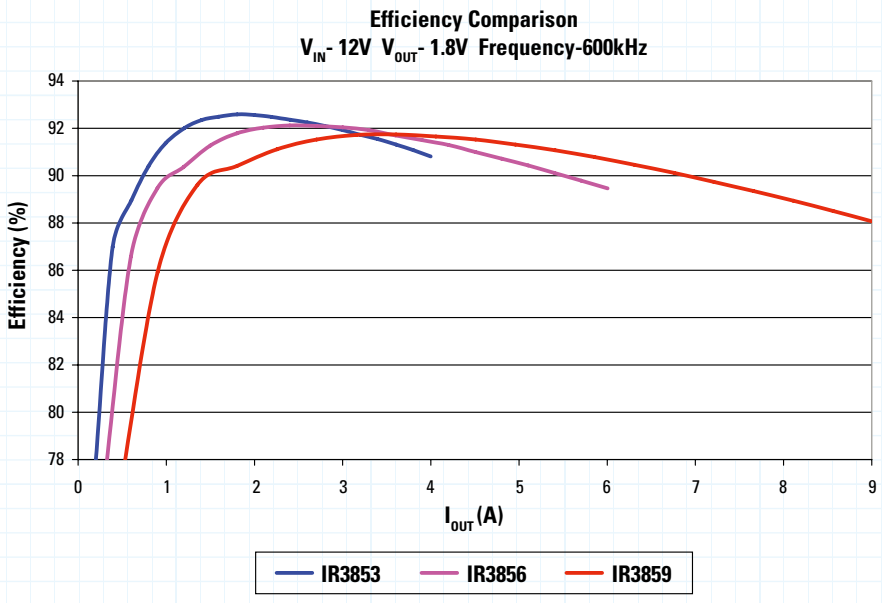
www.powersystemsdesign.com




# 4x5mm Family Shrinks Sup*IR*Buck™ Footprint By 33% Up To 9A

Visit us at PCIM Europe 2011
Hall 12, Stand 202

Sup*IR*Buck™ integrated regulators save energy, space and system cost for your POL design




## Features

- Pin compatible solutions for 4A, 6A, and 9A
- Best in class efficiency over entire load range
- Fully featured and protected for easy on-board implementation
- Wide input voltage range 1.5V to 21V
- Integrated controller, bootstrap diode, control FET and Sync FETKY
- Programmable frequency up to 1.5MHz
- ± 1% accurate 0.7V reference voltage

*Begin your design with IR's online design tool at*
**mypower.irf.com/Sup*IR*Buck**

## Specifications

| Part Number | $I_{OUT}$ (A) | Reference Design |
|---|---|---|
| IR3853M | 4 | IRDC3853 |
| IR3856M | 6 | IRDC3856 |
| IR3859M | 9 | IRDC3859 |

**for more information call +49 (0) 6102 884 311 or visit us at www.irf.com**

International IOR Rectifier
THE POWER MANAGEMENT LEADER